

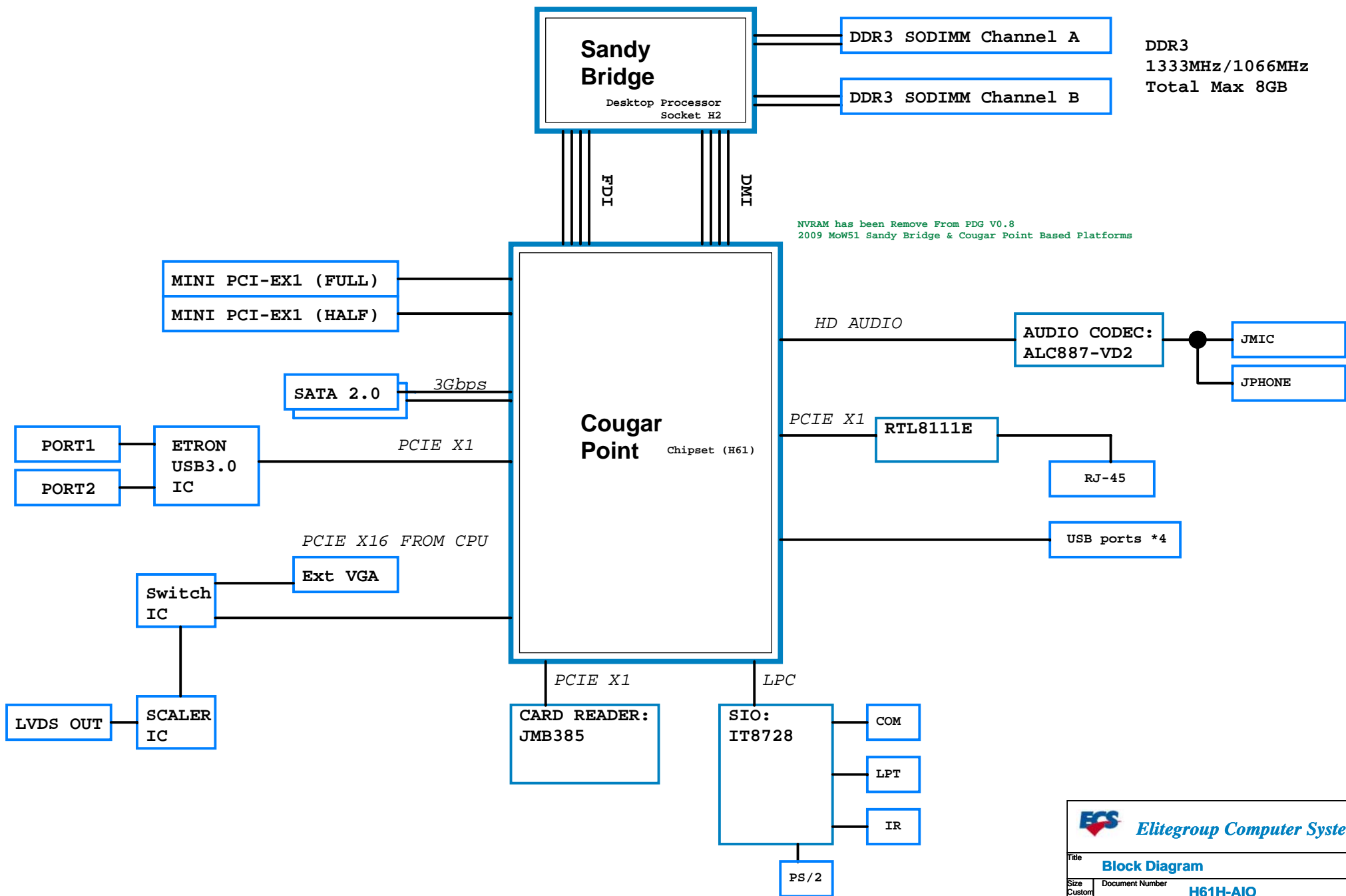


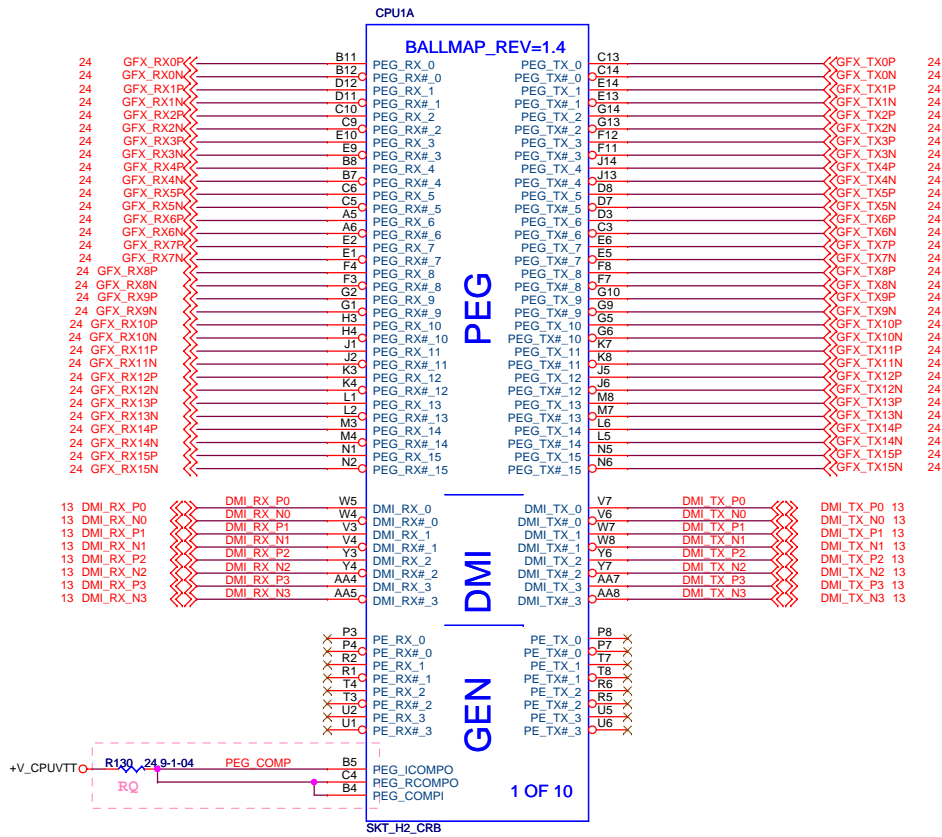
Acer fShenzhen AIO

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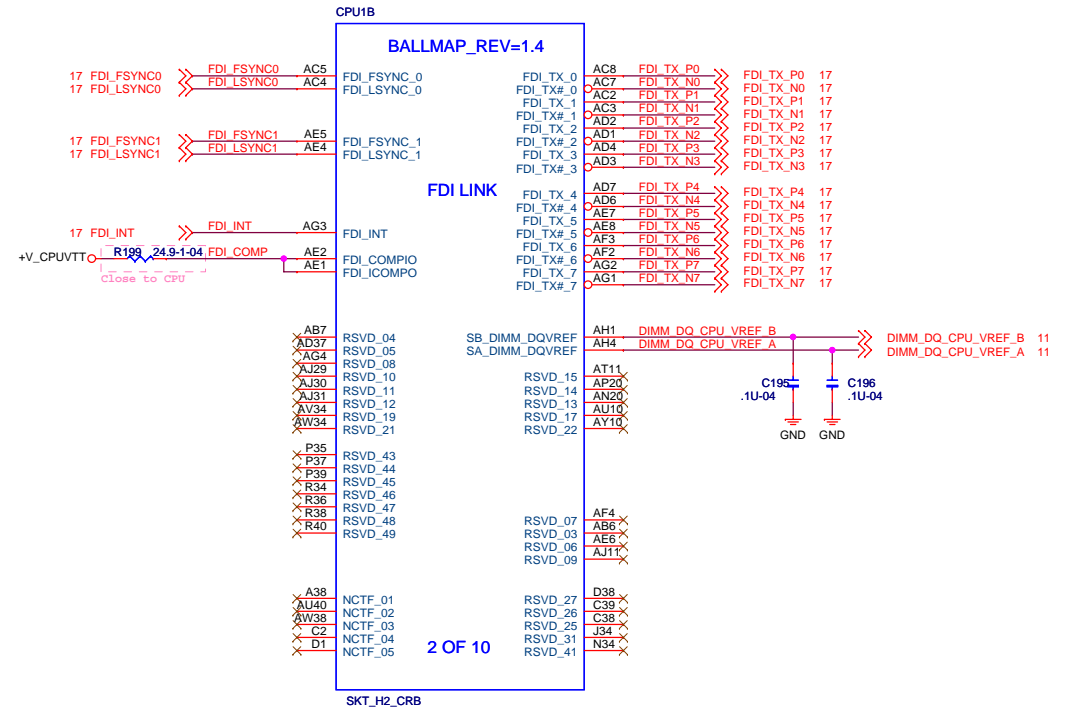
REVISION HISTORY:

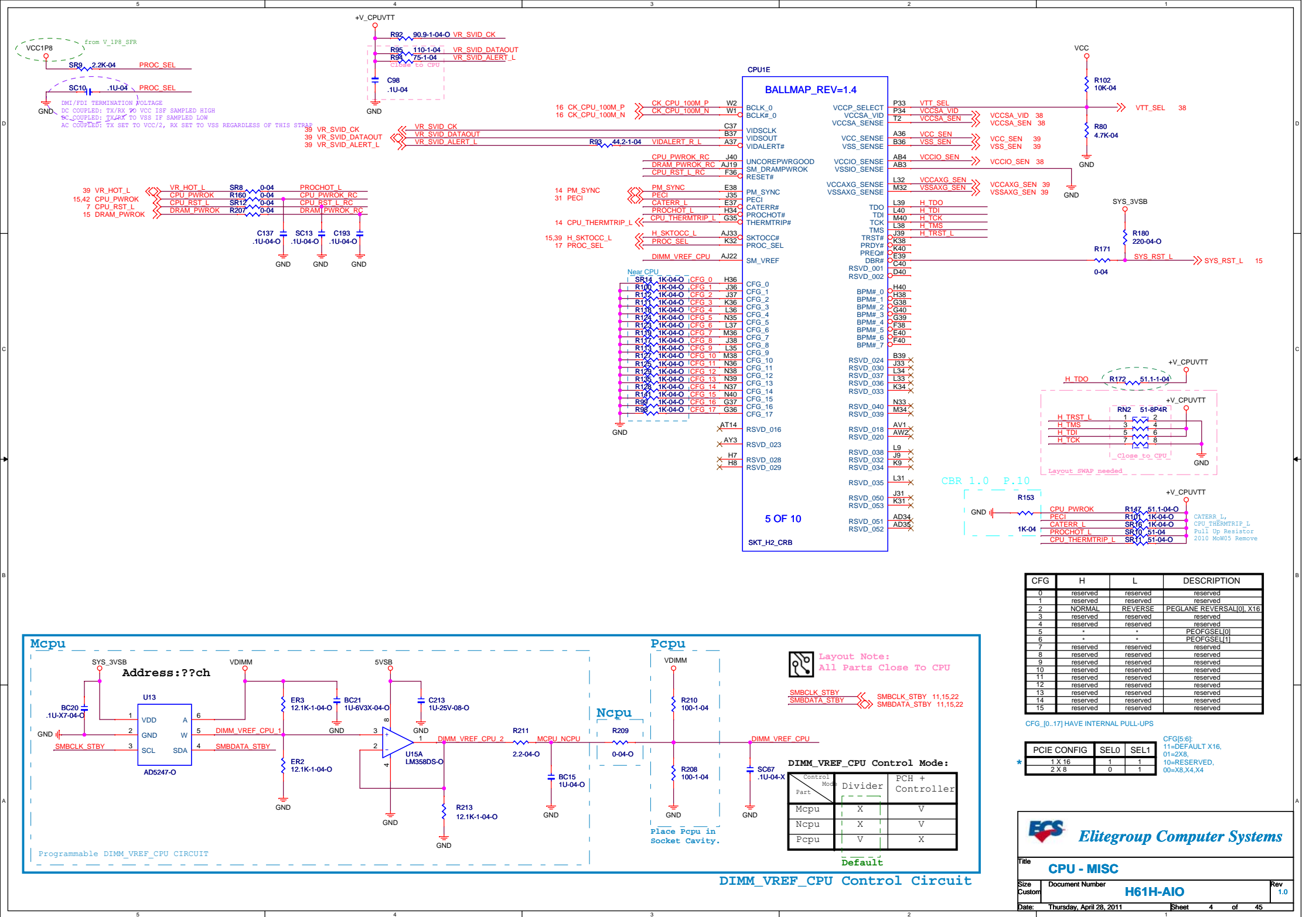
Rev : 1.0

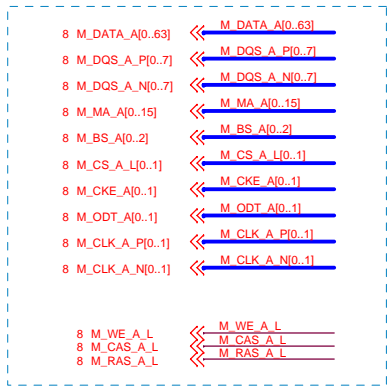




SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4MIL TRACE TO RQ.
1 ROUTE B5 TO RQ. 1 AS A SEPERATE 12MIL TRACE.

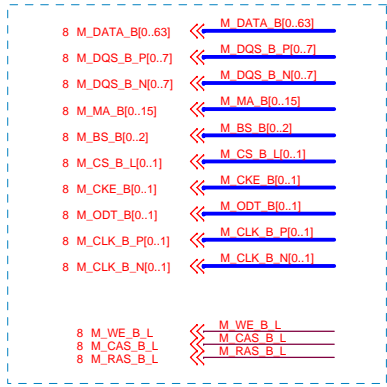




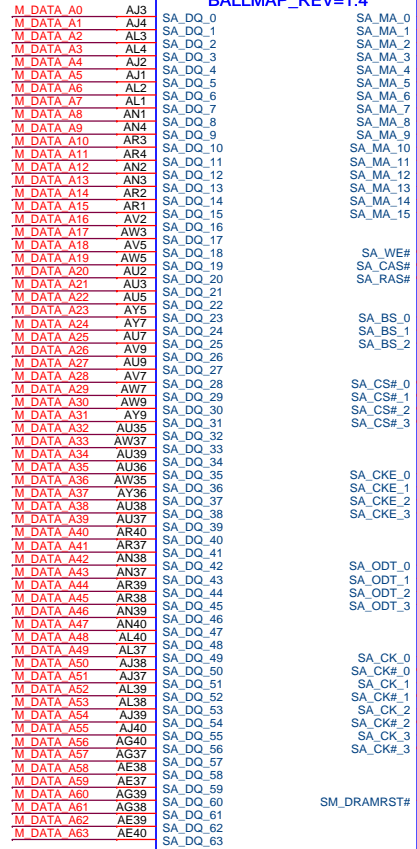


DDR3 CH.A

8 DDR3_DRAMRST_L << DDR3_DRAMRST_L



DDR3 CH.B



SM_DRAMRST#

SA_DQS_8

SA_DQS_8

SA_ECC_CB_0

SA_ECC_CB_1

SA_ECC_CB_2

SA_ECC_CB_3

SA_ECC_CB_4

SA_ECC_CB_5

SA_ECC_CB_6

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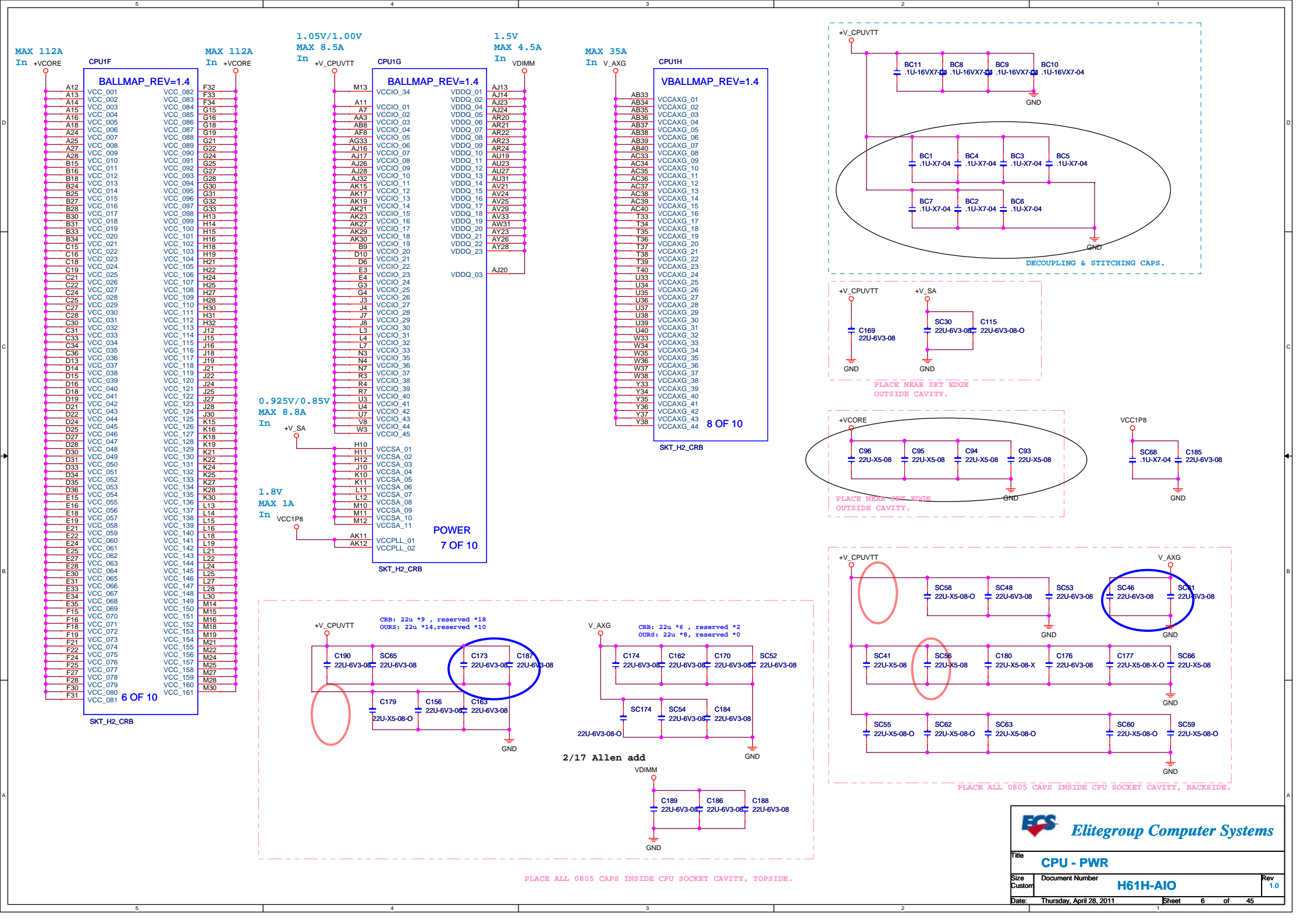
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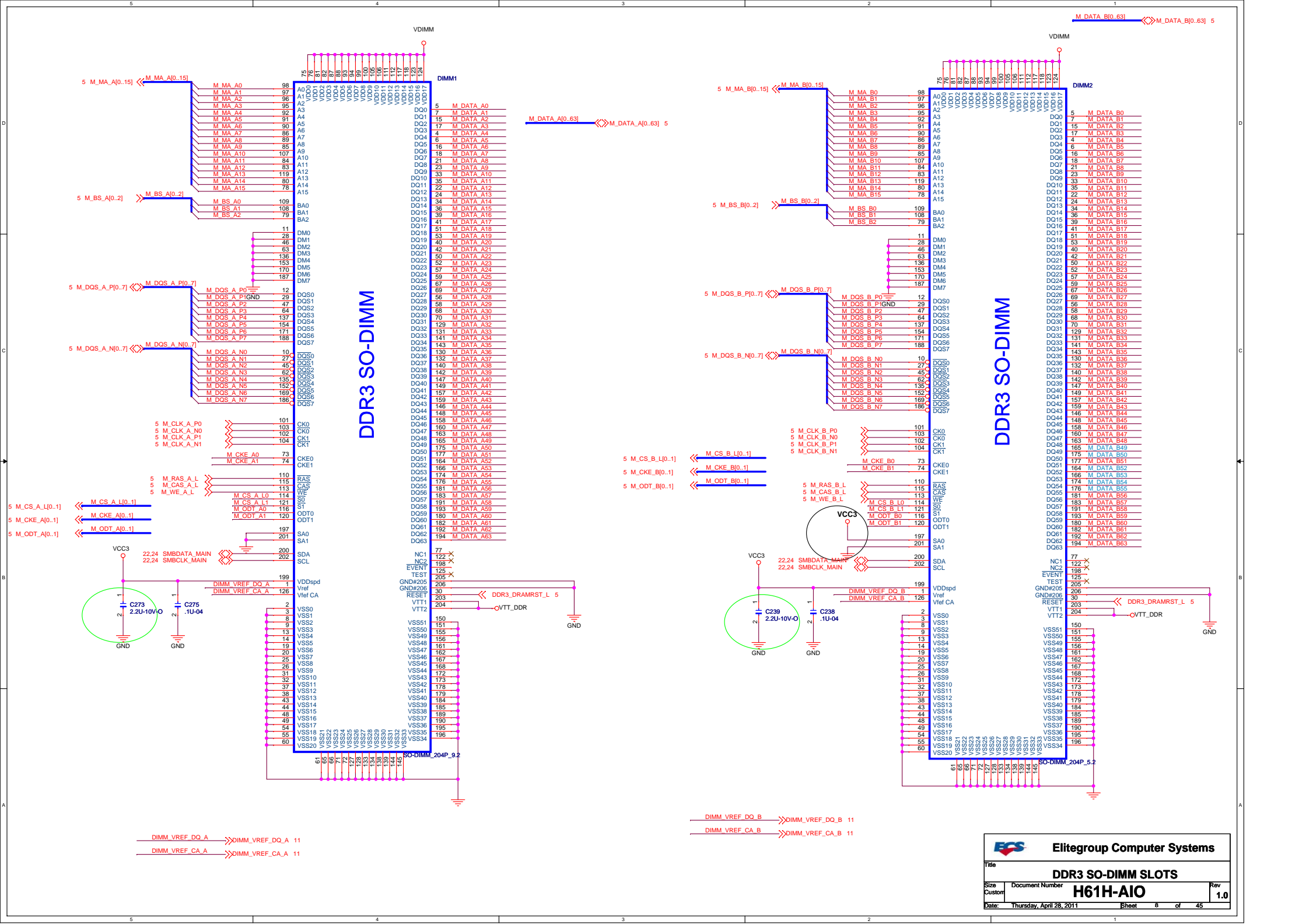
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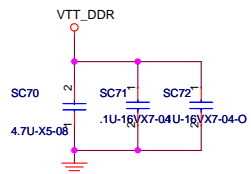
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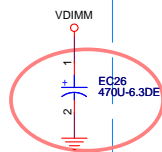
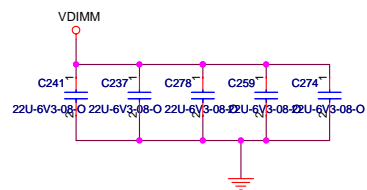
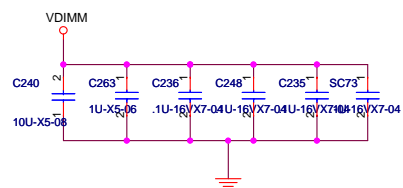


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A23	VSS_002	VSS_092	AM3	AV17	VSS_183	VSS_273	H17			AV17	VSS_183	VSS_273	H17						
A26	VSS_003	VSS_093	AM30	AV3	VSS_184	VSS_274	H2			AV35	VSS_185	VSS_275	H20						
AA29	VSS_004	VSS_094	AM36	AV38	VSS_186	VSS_276	H26			AV38	VSS_186	VSS_276	H26						
AA33	VSS_005	VSS_095	AM37	AV6	VSS_187	VSS_277	H29			AV6	VSS_187	VSS_277	H29						
AA34	VSS_006	VSS_096	AM38	AW10	VSS_188	VSS_278	H33			AW10	VSS_188	VSS_278	H33						
AA35	VSS_007	VSS_097	AM4	AW11	VSS_189	VSS_279	H35			AW11	VSS_189	VSS_279	H35						
AA36	VSS_008	VSS_098	AM40	AW16	VSS_190	VSS_280	H37			AW16	VSS_190	VSS_280	H37						
AA37	VSS_009	VSS_099	AM5	AW36	VSS_191	VSS_281	H39			AW36	VSS_191	VSS_281	H39						
AA38	VSS_010	VSS_100	AN10	AW6	VSS_192	VSS_282	H5			AW6	VSS_192	VSS_282	H5						
AA6	VSS_011	VSS_101	AN11	AY11	VSS_193	VSS_283	H6			AY11	VSS_193	VSS_283	H6						
AB5	VSS_012	VSS_102	AN14	AY14	VSS_194	VSS_284	H9			AY14	VSS_194	VSS_284	H9						
AC1	VSS_013	VSS_103	AN17	AY18	VSS_195	VSS_285	J11			AY18	VSS_195	VSS_285	J11						
AC6	VSS_014	VSS_104	AN19	AY35	VSS_196	VSS_286	J17			AY35	VSS_196	VSS_286	J17						
AD33	VSS_015	VSS_105	AN22	AY4	VSS_197	VSS_287	J20			AY4	VSS_197	VSS_287	J20						
AD36	VSS_016	VSS_106	AN24	AY6	VSS_198	VSS_288	J23			AY6	VSS_198	VSS_288	J23						
AD38	VSS_017	VSS_107	AN27	AY8	VSS_199	VSS_289	J26			AY8	VSS_199	VSS_289	J26						
AD39	VSS_018	VSS_108	AN30	B10	VSS_200	VSS_290	J29			B10	VSS_200	VSS_290	J29						
AD40	VSS_019	VSS_109	AN33	B17	VSS_201	VSS_291	J32			B17	VSS_201	VSS_291	J32						
AD5	VSS_020	VSS_110	AN32	B23	VSS_202	VSS_292	K1			B23	VSS_202	VSS_292	K1						
AD8	VSS_021	VSS_111	AN33	B29	VSS_203	VSS_293	K12			B29	VSS_203	VSS_293	K12						
AE3	VSS_022	VSS_112	AN34	B32	VSS_204	VSS_294	K13			B32	VSS_204	VSS_294	K13						
AE33	VSS_023	VSS_113	AN35	B35	VSS_205	VSS_295	K14			B35	VSS_205	VSS_295	K14						
AE36	VSS_024	VSS_114	AN36	B38	VSS_206	VSS_296	K17			B38	VSS_206	VSS_296	K17						
AF1	VSS_025	VSS_115	AN5	B6	VSS_207	VSS_297	K2			B6	VSS_207	VSS_297	K2						
AF34	VSS_026	VSS_116	AN7	B6	VSS_208	VSS_298	K20			AN7	VSS_208	VSS_298	K20						
AF36	VSS_027	VSS_117	AN8	B6	VSS_209	VSS_299	K23			AN8	VSS_209	VSS_299	K23						
AF37	VSS_028	VSS_118	AN9	B6	VSS_210	VSS_300	K26			AN9	VSS_210	VSS_300	K26						
AF40	VSS_029	VSS_119	AP1	C11	VSS_211	VSS_301	K29			AP1	VSS_211	VSS_301	K29						
AF5	VSS_030	VSS_120	AP11	C12	VSS_212	VSS_302	K33			AP11	VSS_212	VSS_302	K33						
AF6	VSS_031	VSS_121	AP14	C17	VSS_213	VSS_303	K35			AP14	VSS_213	VSS_303	K35						
AF7	VSS_032	VSS_122	AP17	C20	VSS_214	VSS_304	K37			AP17	VSS_214	VSS_304	K37						
AG36	VSS_033	VSS_123	AP22	C23	VSS_215	VSS_305	K39			AP22	VSS_215	VSS_305	K39						
AH2	VSS_034	VSS_124	AP25	C26	VSS_216	VSS_306	K5			AP25	VSS_216	VSS_306	K5						
AH3	VSS_035	VSS_125	AP27	C29	VSS_217	VSS_307	K6			AP27	VSS_217	VSS_307	K6						
AH33	VSS_036	VSS_126	AP30	C32	VSS_218	VSS_308	L10			AP30	VSS_218	VSS_308	L10						
AH37	VSS_037	VSS_127	AP36	C35	VSS_219	VSS_309	L17			AP36	VSS_219	VSS_309	L17						
AH38	VSS_038	VSS_128	AP37	C7	VSS_220	VSS_310	L20			AP37	VSS_220	VSS_310	L20						
AH39	VSS_039	VSS_129	AP4	D2	VSS_221	VSS_311	L23			AP4	VSS_221	VSS_311	L23						
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AH8	VSS_042	VSS_132	AR11	D20	VSS_224	VSS_314	L8			AR11	VSS_224	VSS_314	L8						
AJ12	VSS_043	VSS_133	AR14	D23	VSS_225	VSS_315	M1			AR14	VSS_225	VSS_315	M1						
AJ15	VSS_044	VSS_134	AR17	D26	VSS_226	VSS_316	M17			AR17	VSS_226	VSS_316	M17						
AJ18	VSS_045	VSS_135	AR18	D29	VSS_227	VSS_317	M2			AR18	VSS_227	VSS_317	M2						
AJ21	VSS_046	VSS_136	AR19	D32	VSS_228	VSS_319	M20			AR19	VSS_228	VSS_319	M20						
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AJ27	VSS_048	VSS_138	AR30	D37	VSS_230	VSS_321	M26			AR30	VSS_230	VSS_321	M26						
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AK35	VSS_063	VSS_153	AT30	F10	VSS_245	VSS_336	P6			AT30	VSS_245	VSS_336	P6						
AK36	VSS_064	VSS_154	AT31	F13	VSS_246	VSS_337	R33			AT31	VSS_246	VSS_337	R33						
AK37	VSS_065	VSS_155	AT32	F14	VSS_247	VSS_338	R35			AT32	VSS_247	VSS_338	R35						
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AK40	VSS_067	VSS_157	AT34	F2	VSS_249	VSS_340	R39			AT34	VSS_249	VSS_340	R39						
AK5	VSS_068	VSS_158	AT35	F20	VSS_250	VSS_341	R8			AT35	VSS_250	VSS_341	R8						
AK6	VSS_069	VSS_159	AT36	F23	VSS_251	VSS_342	T1			AT36	VSS_251	VSS_342	T1						
AK7	VSS_070	VSS_160	AT37	F26	VSS_252	VSS_343	T5			AT37	VSS_252	VSS_343	T5						
AK8	VSS_071	VSS_161	AT38	F29	VSS_253	VSS_344	T6			AT38	VSS_253	VSS_344	T6						
AK9	VSS_072	VSS_162	AT39	F35	VSS_254	VSS_345	U8			AT39	VSS_254	VSS_345	U8						
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AL27	VSS_078	VSS_168	AT8	G11	VSS_260	VSS_351	V36			AT8	VSS_260	VSS_351	V36						
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AM11	VSS_084	VSS_174	AT34	G29	VSS_266	VSS_357	W6			AM11	VSS_266	VSS_357	W6						
AM14	VSS_085	VSS_175	AT34	G34	VSS_267	VSS_358	Y5			AM14	VSS_267	VSS_358	Y5						
AM17	VSS_086	VSS_176	AT34</																

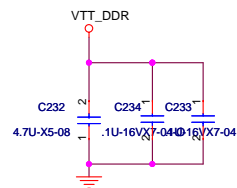




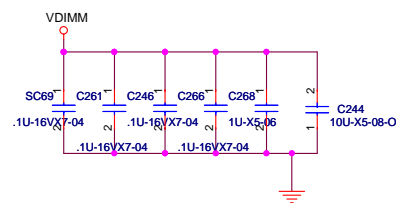
Layout: Close to DIMM0



3/3 allen ch bom

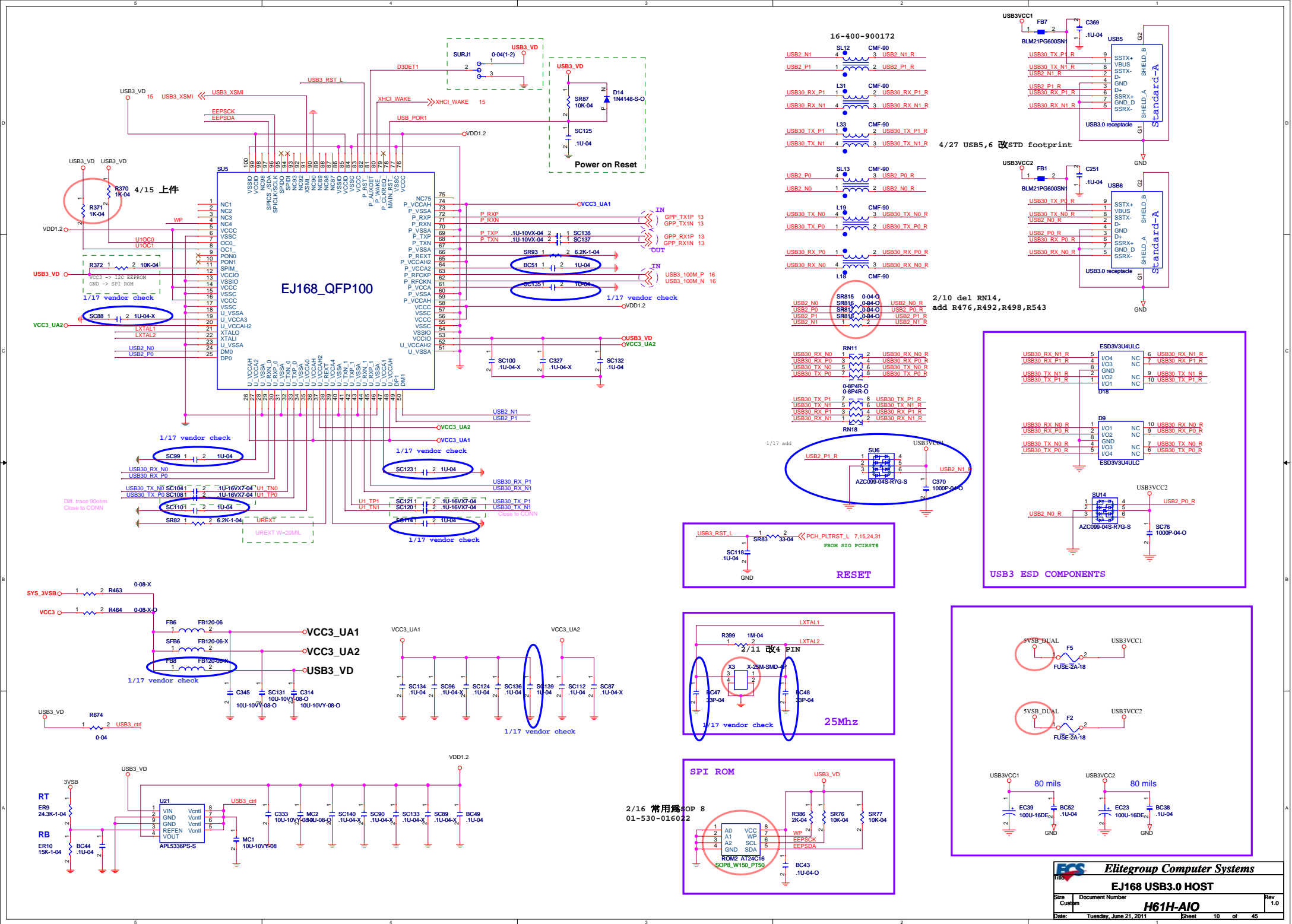


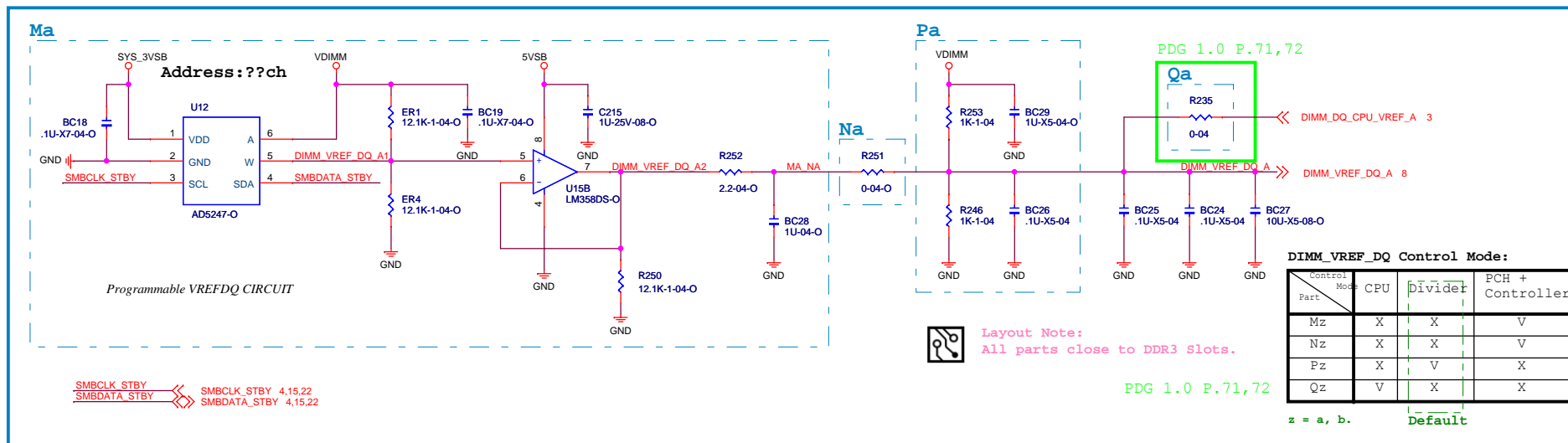
Layout: Close to DIMM1



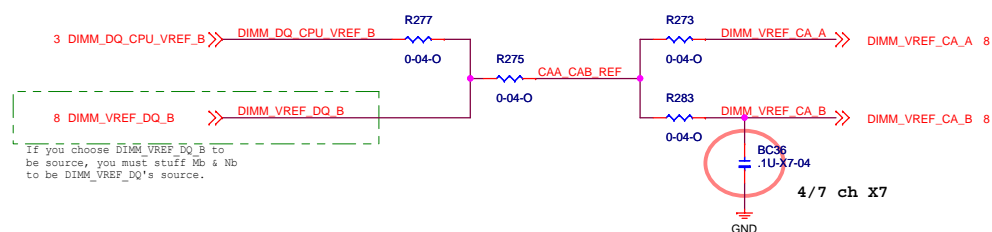
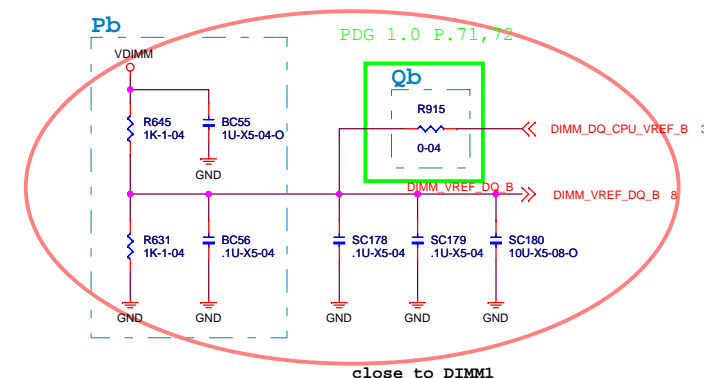
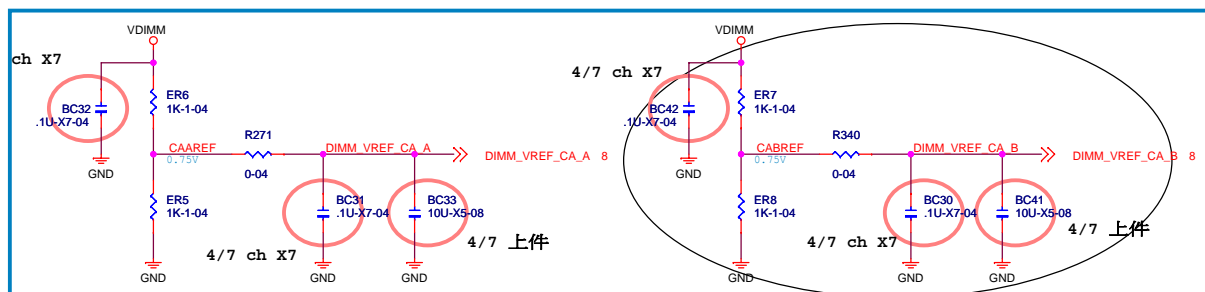
Elitegroup Computer Systems

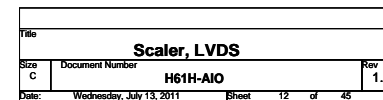
Title			DDR3 SODIMM CAPACITOR
Size			Custom
Document Number			H61H-AIO
Date:			Tuesday, May 17, 2011
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Rev			1.0

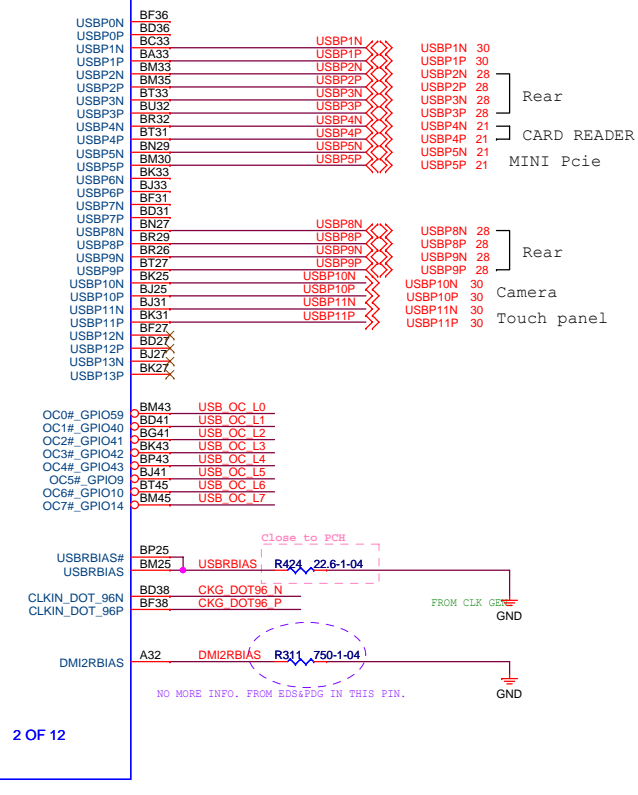
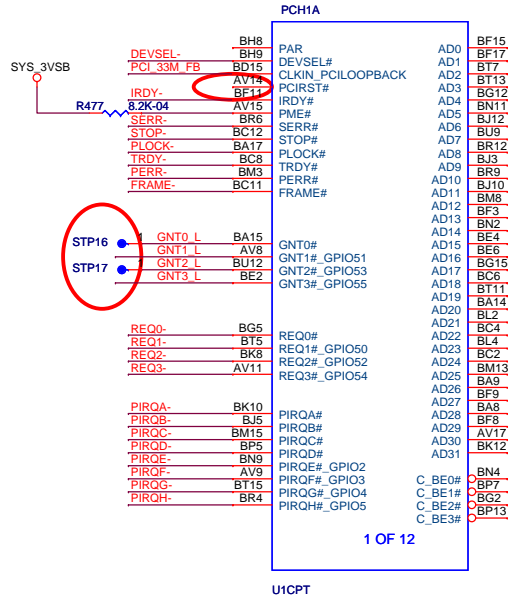
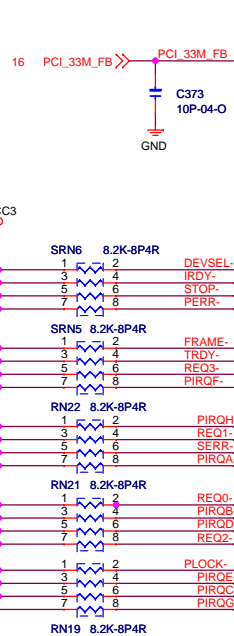




DIMM_VREF_DQ Control Circuit





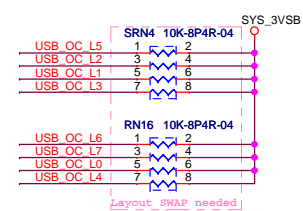
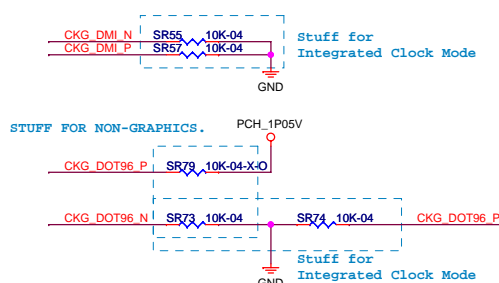
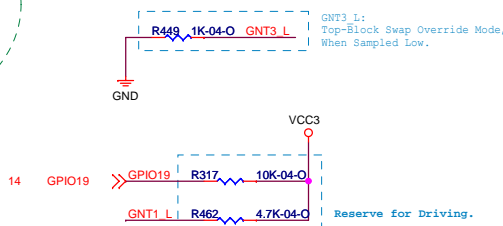


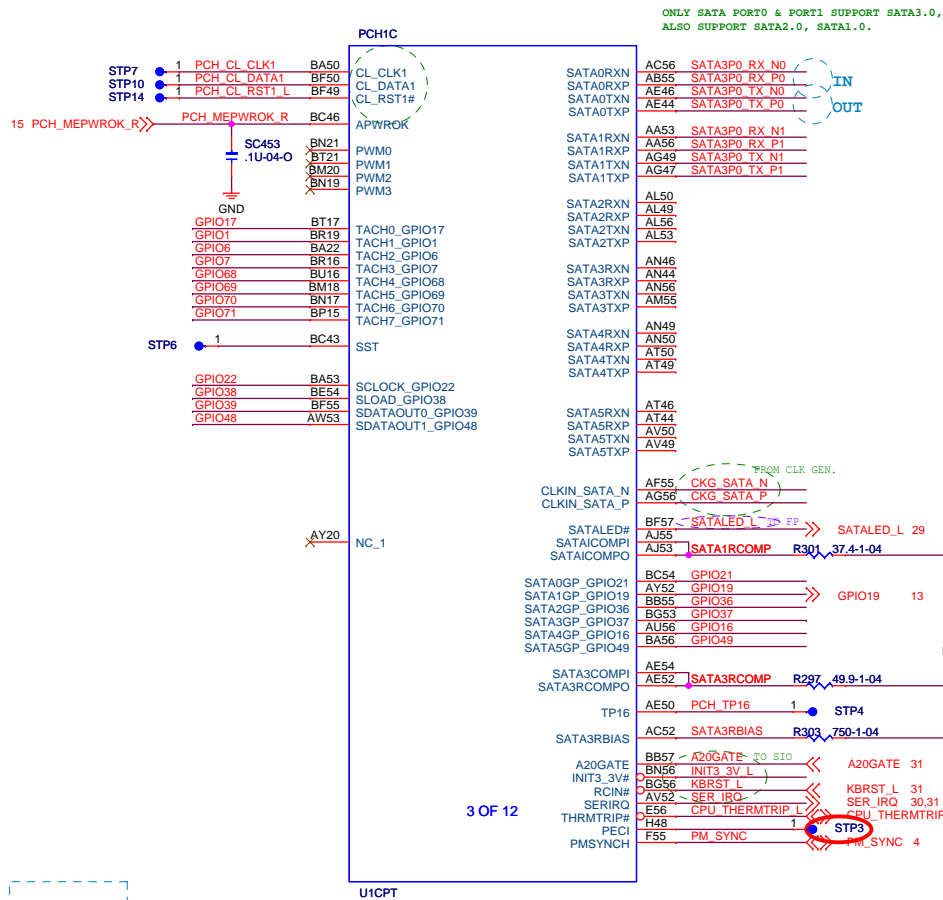
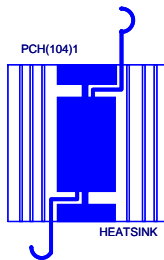
Boot Device Select:

BOOT DEVICE	GNT1_L	GPI019
LPC	0	0
PCI	1	0
SPI	1	1

GNT1[0..3]#
GPI019
have been internal pull high to +VCC3

GNT1#, GPI019 Follow CPT EDS V0.7,
CRB V0.7, PDG V0.8



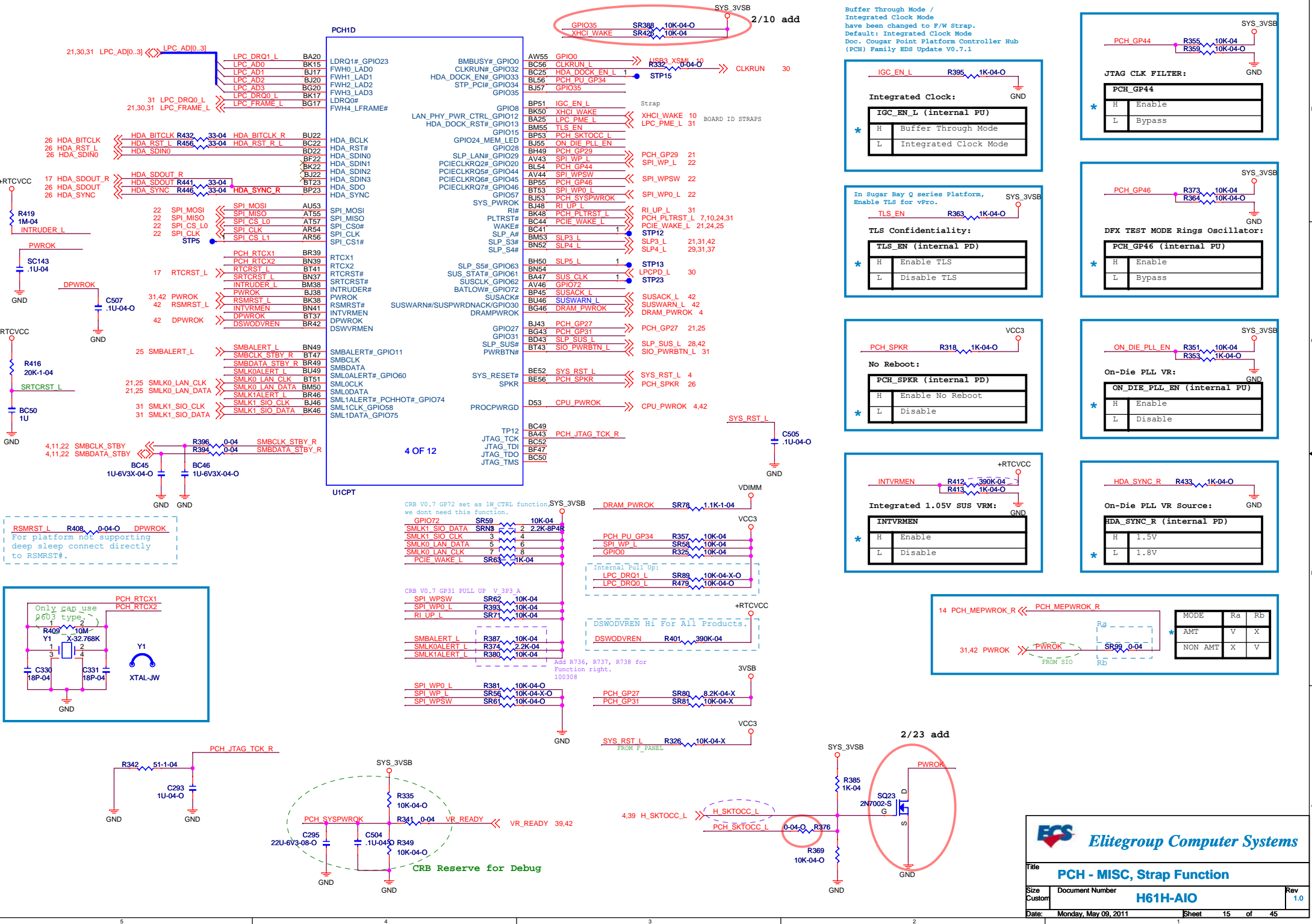


2/1 ch pull down to pull high



Elitegroup Computer Systems

Title			PCH - SATA, SATA CONN
Size	Document Number	H61H-AIO	
Custom		Rev 1.0	
Date:	Monday, May 09, 2011	Sheet	14 of 45



Buffer Through Mode / Integrated Clock Mode have been changed to F/W Strap. Default: Integrated Clock Mode Doc, Cougar Point Platform Controller Hub (PCH) Family EDS Update V0.7.1

JTAG CLK FILTER:

PCH_GP44

H	Enable
L	Bypass

DFX TEST MODE Rings Oscillator:

PCH_GP46 (internal PU)

H	Enable
L	Bypass

On-Die PLL VR:

ON_DIE_PLL_EN (internal PU)

H	Enable
L	Disable

On-Die PLL VR Source:

HDA_SYNC_R (internal PD)

H	1.5V
L	1.8V

Integrated Clock:

IGC_EN_L (internal PU)

H	Buffer Through Mode
L	Integrated Clock Mode

TLS Confidentiality:

TLS_EN (internal PD)

H	Enable TLS
L	Disable TLS

No Reboot:

PCH_SPKR (internal PD)

H	Enable No Reboot
L	Disable

Integrated 1.05V SUS VRM:

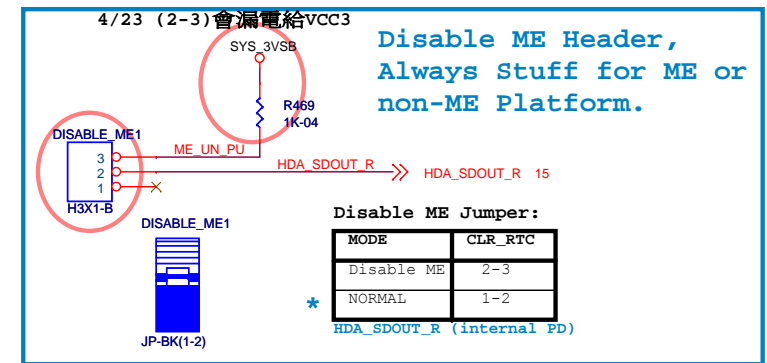
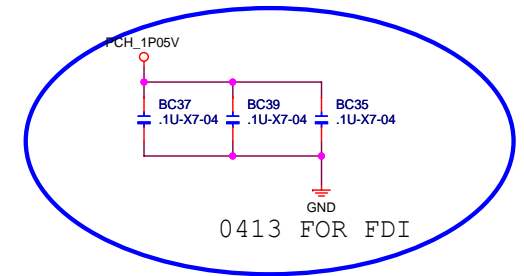
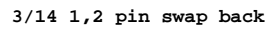
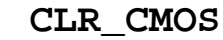
INTVRMEN

H	Enable
L	Disable

14 PCH_MEPWROK_R

MODE

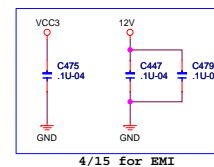
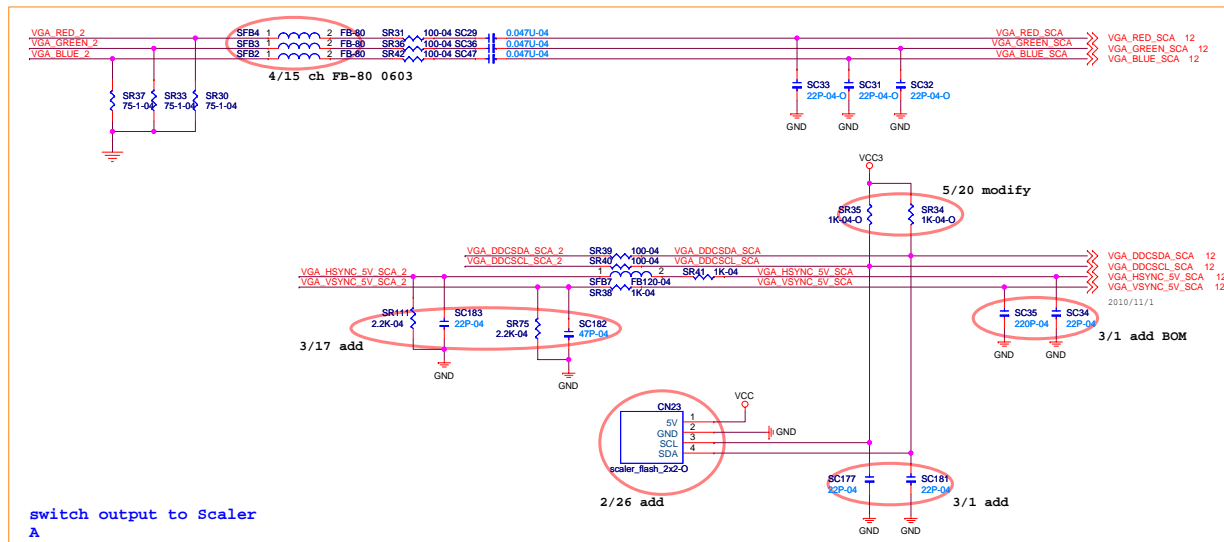
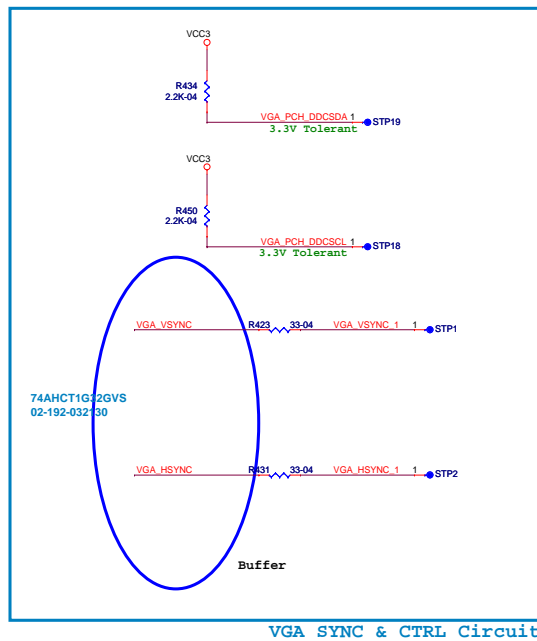
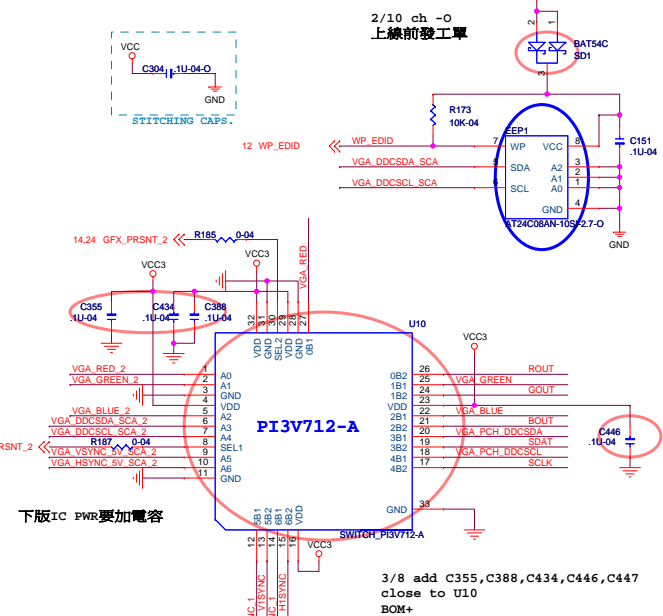
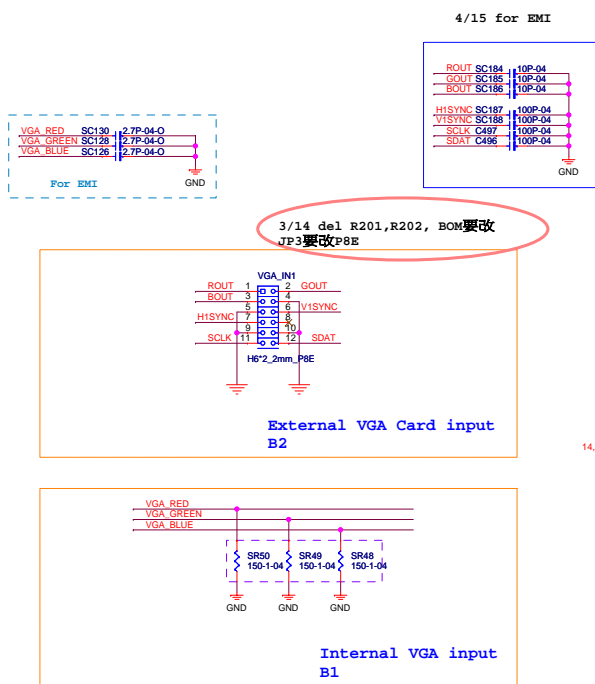
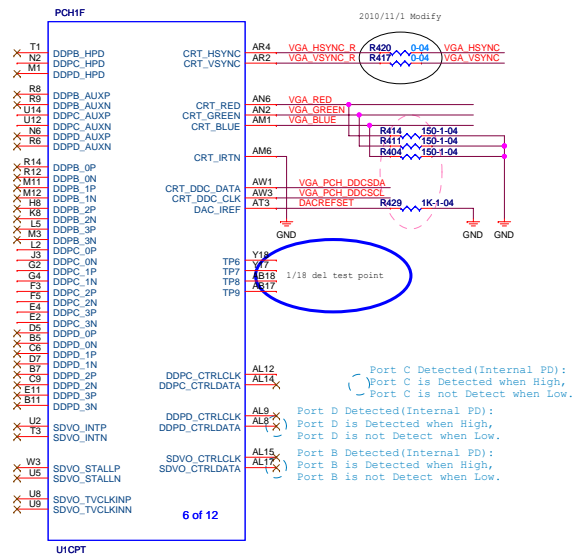
Ra	Rb
AMT	V X
NON AMT	X V

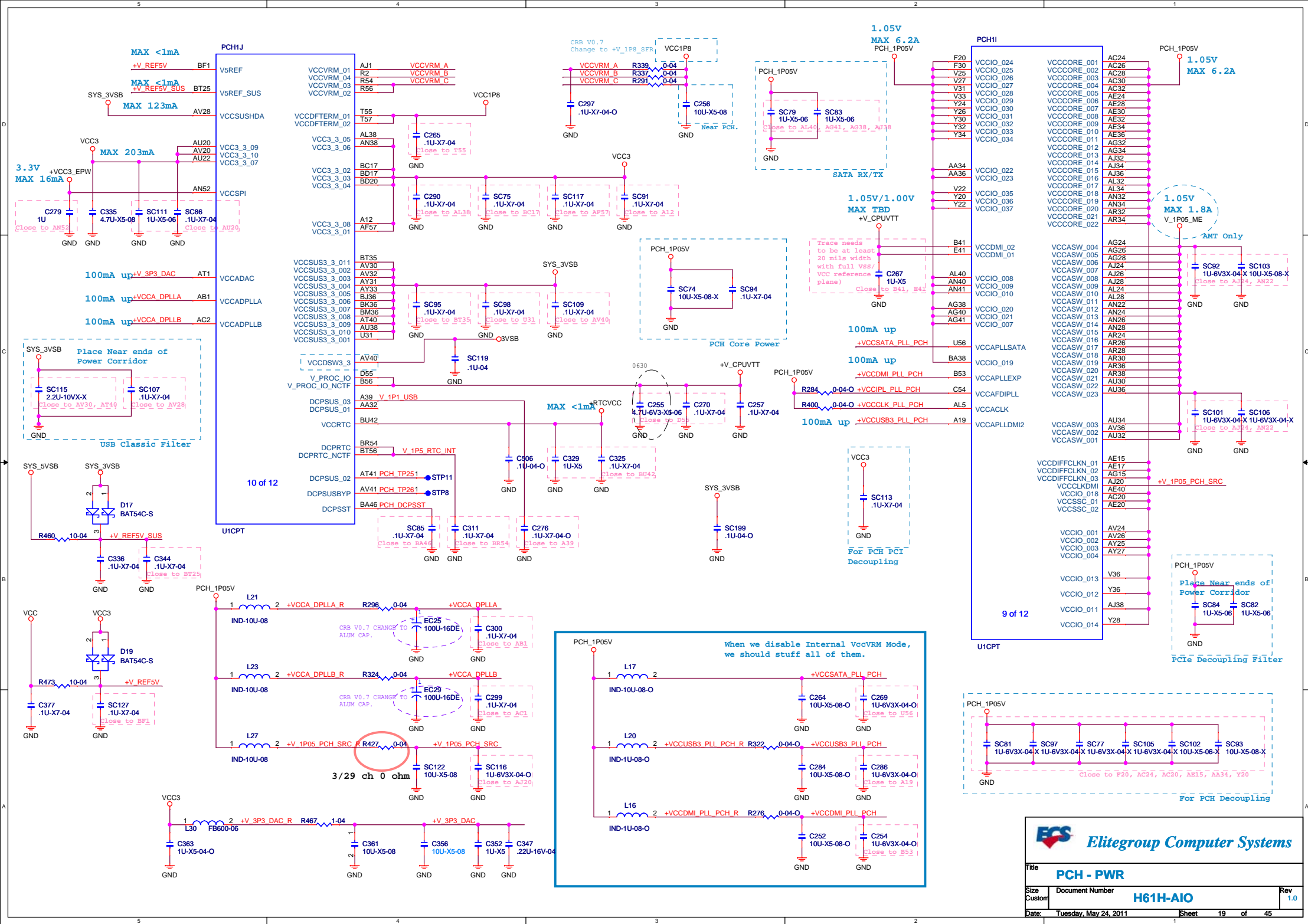
DMI and FDI Tx/
Rx Termination
Voltage

title	PCH - NVRAM/FDI, CLR_CMOS
-------	---------------------------

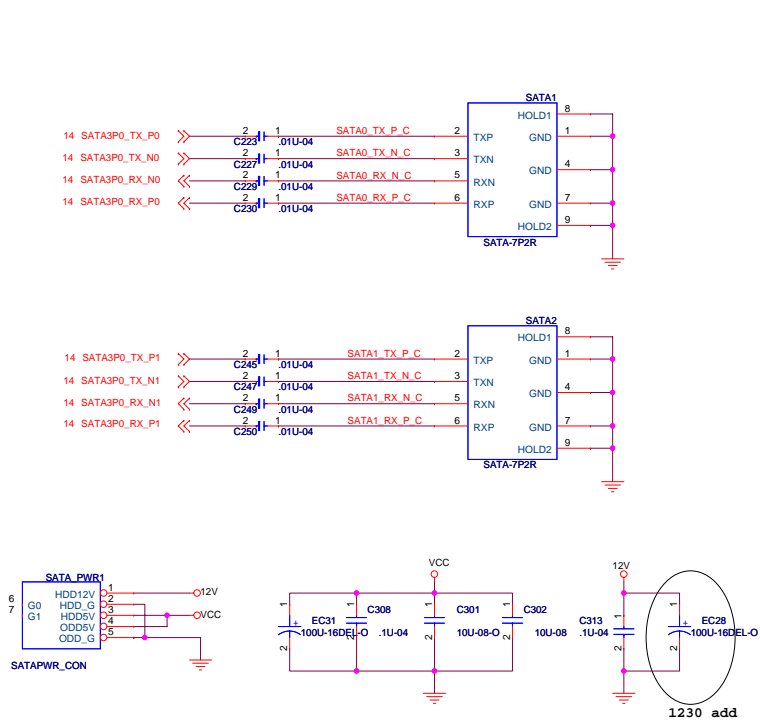
Rev
1.0

Sheet 17 of 45

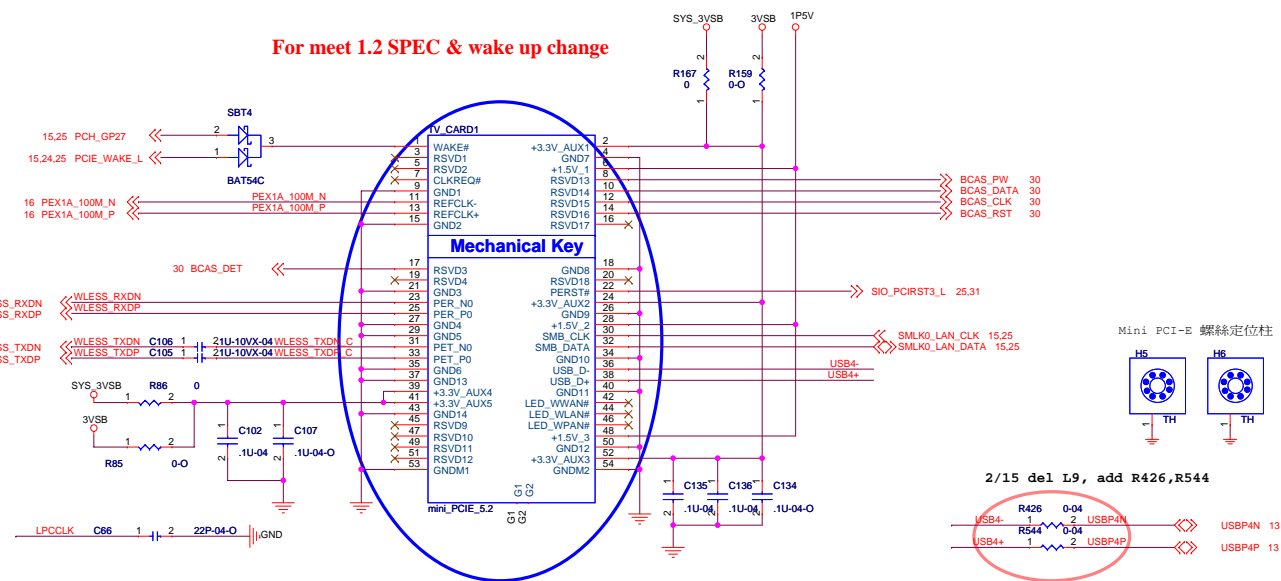




SATA

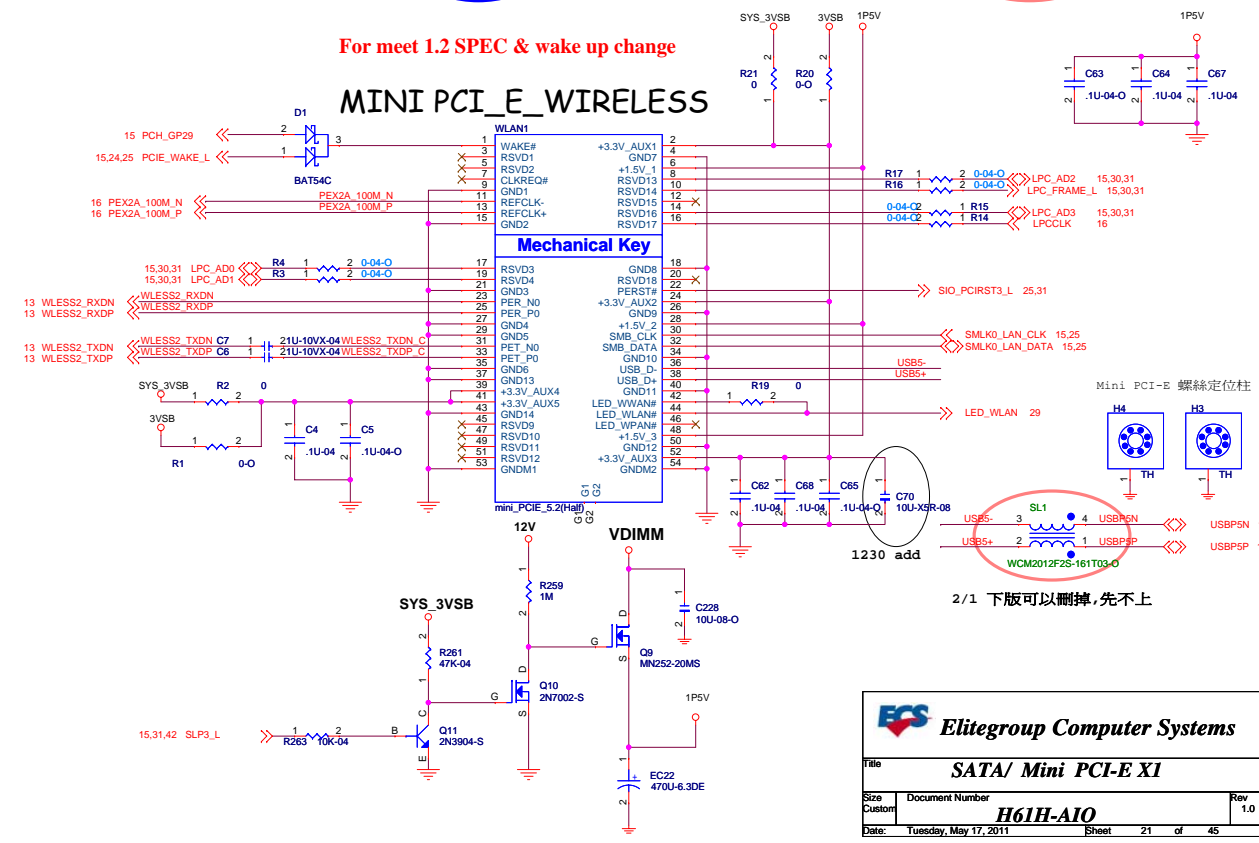


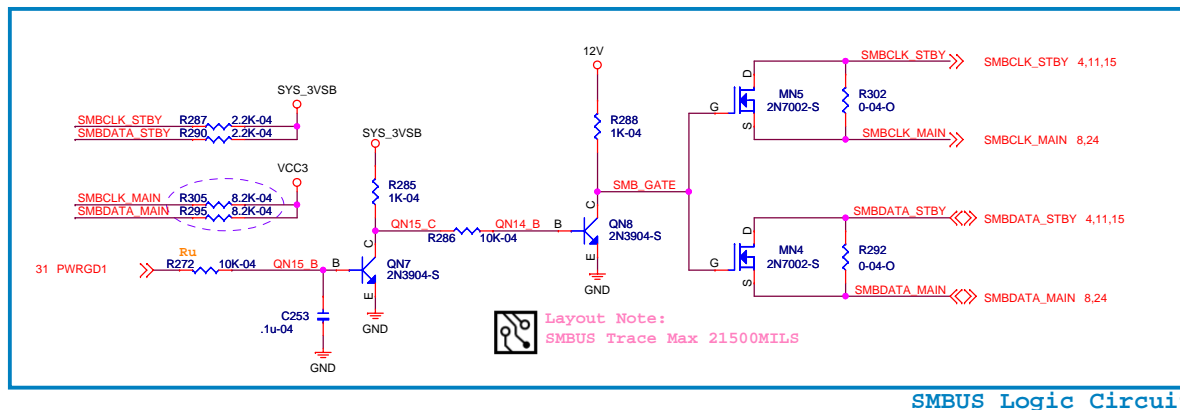
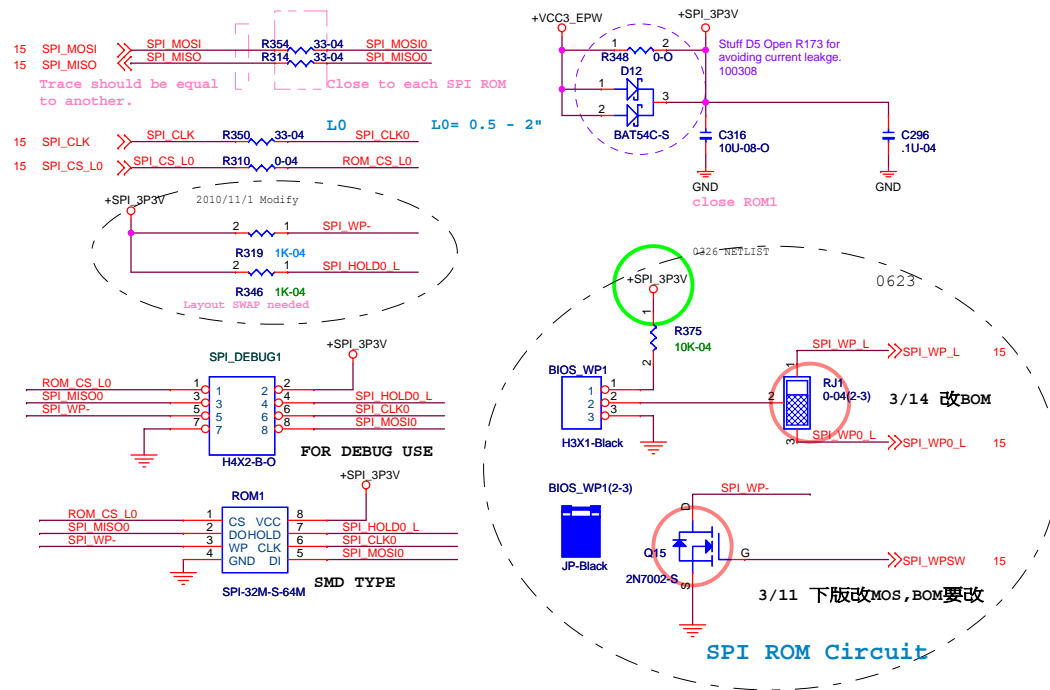
For meet 1.2 SPEC & wake up change

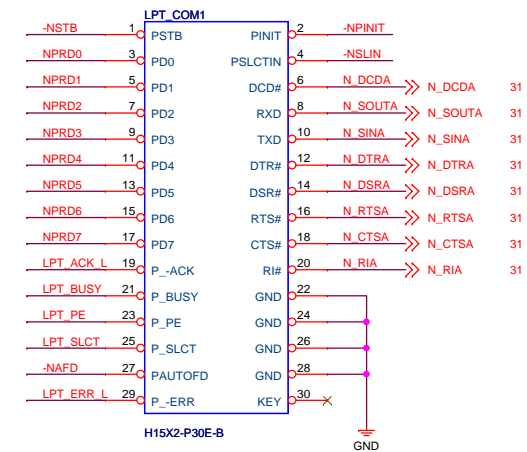
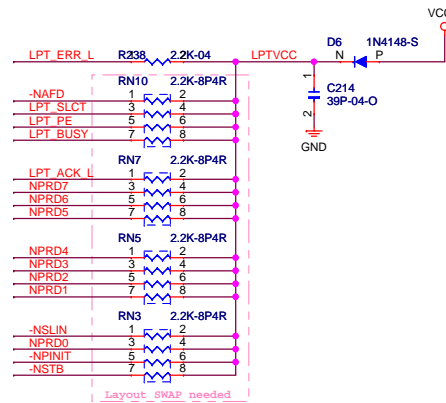
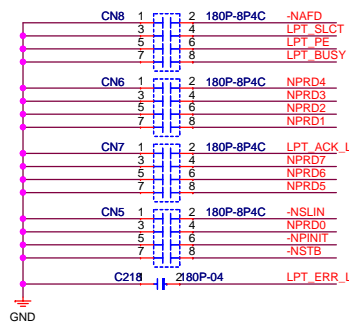
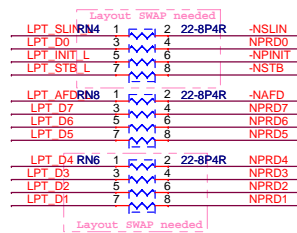
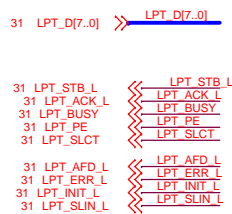


For meet 1.2 SPEC & wake up change


MINI PCI_E_WIRELESS

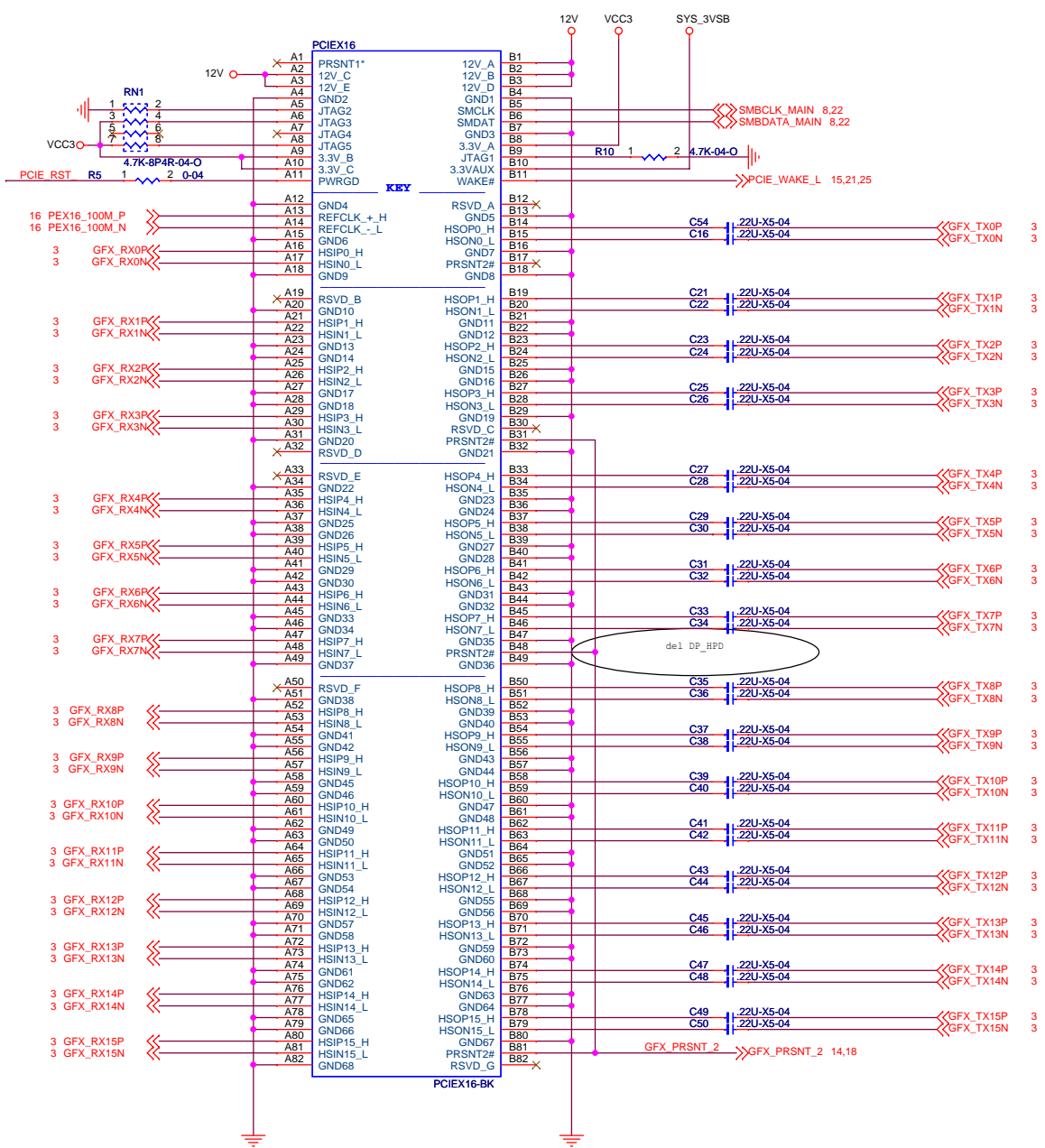




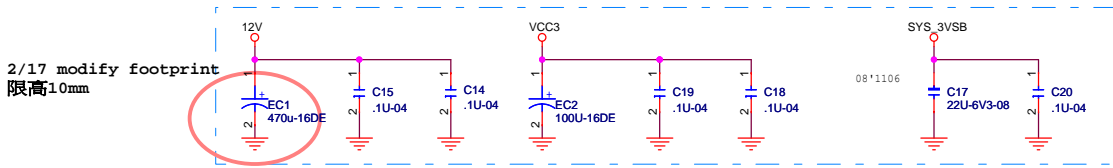


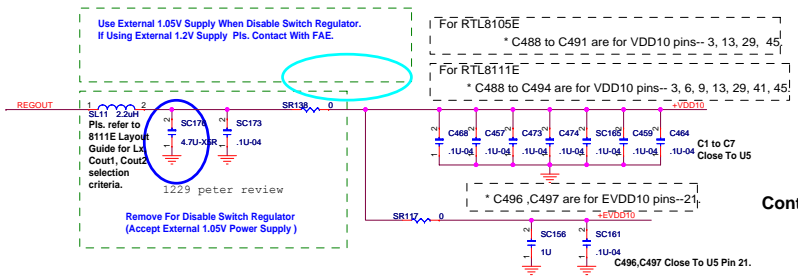
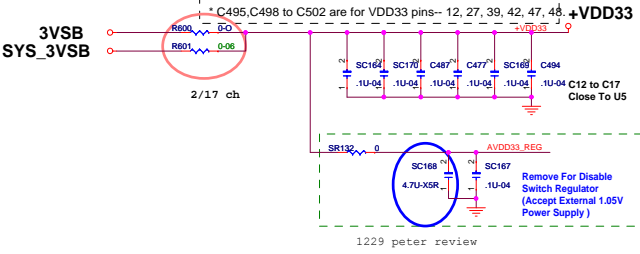
LPT&COM Header Circuit

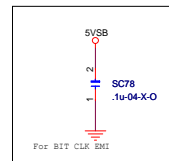
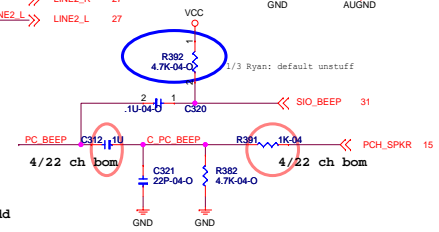
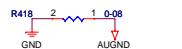
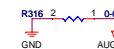
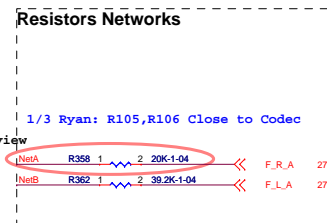
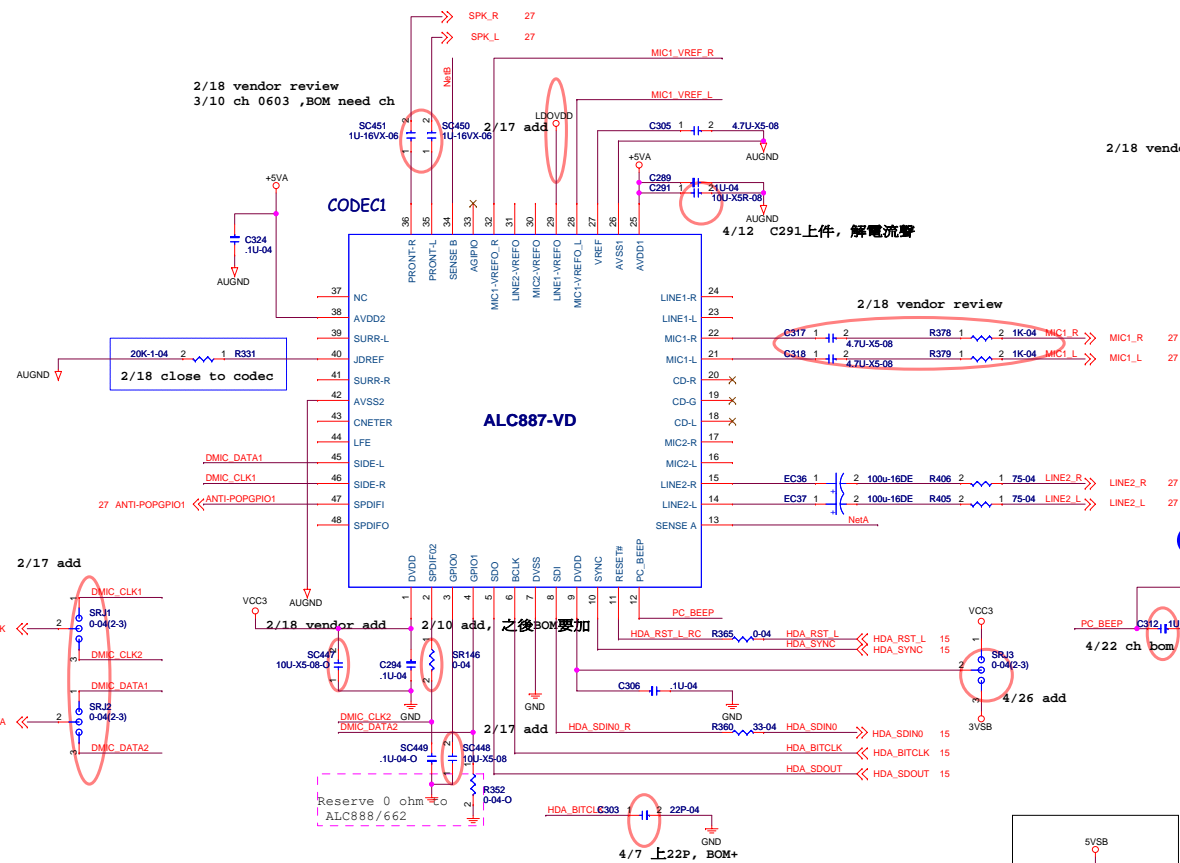
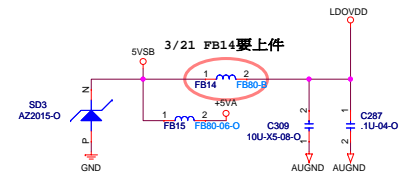
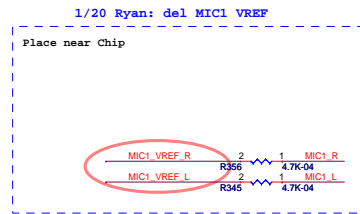
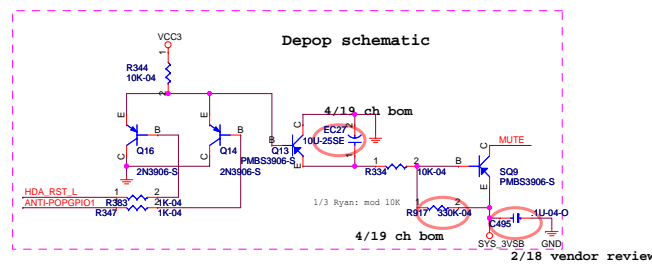
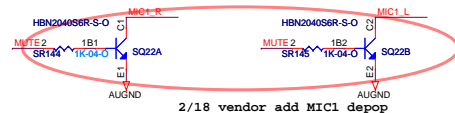
 Elitegroup Computer Systems		
COM/LPT		
Title Size Custom	Document Number H61H-AIO	Rev 1.0
Date: Thursday, June 16, 2011 Sheet 23 of 45		

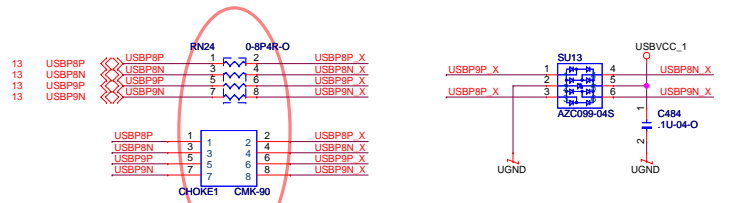


Please place the caps close to PCIe16 Slot.

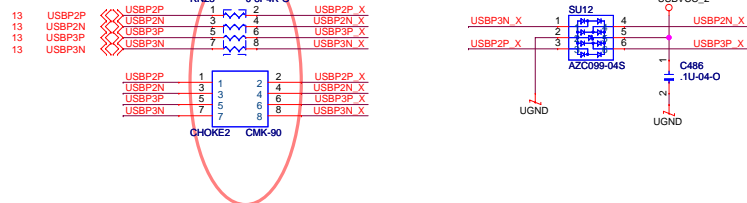




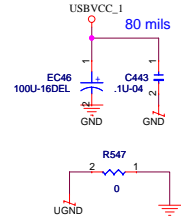
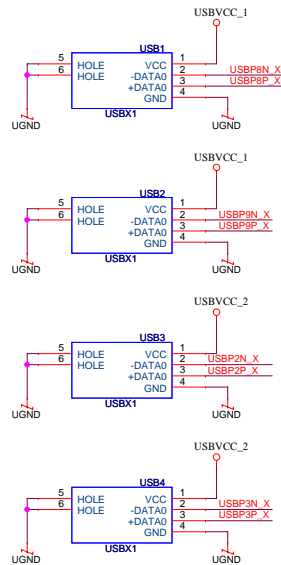




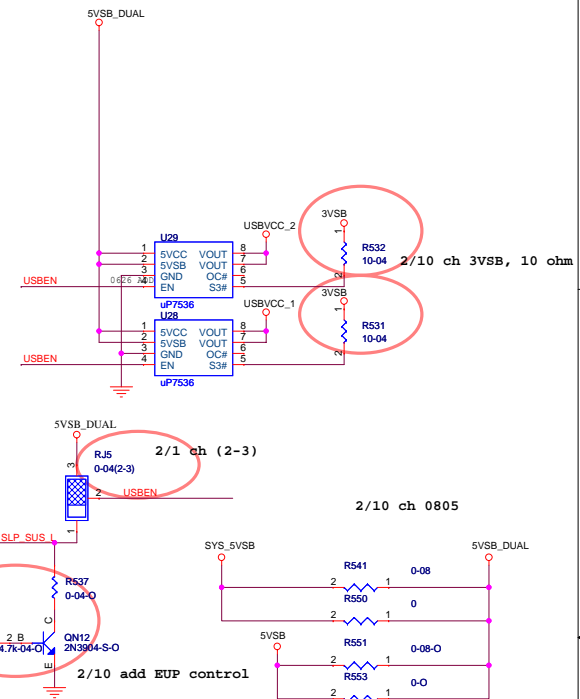
2/1 ch 0 ohm



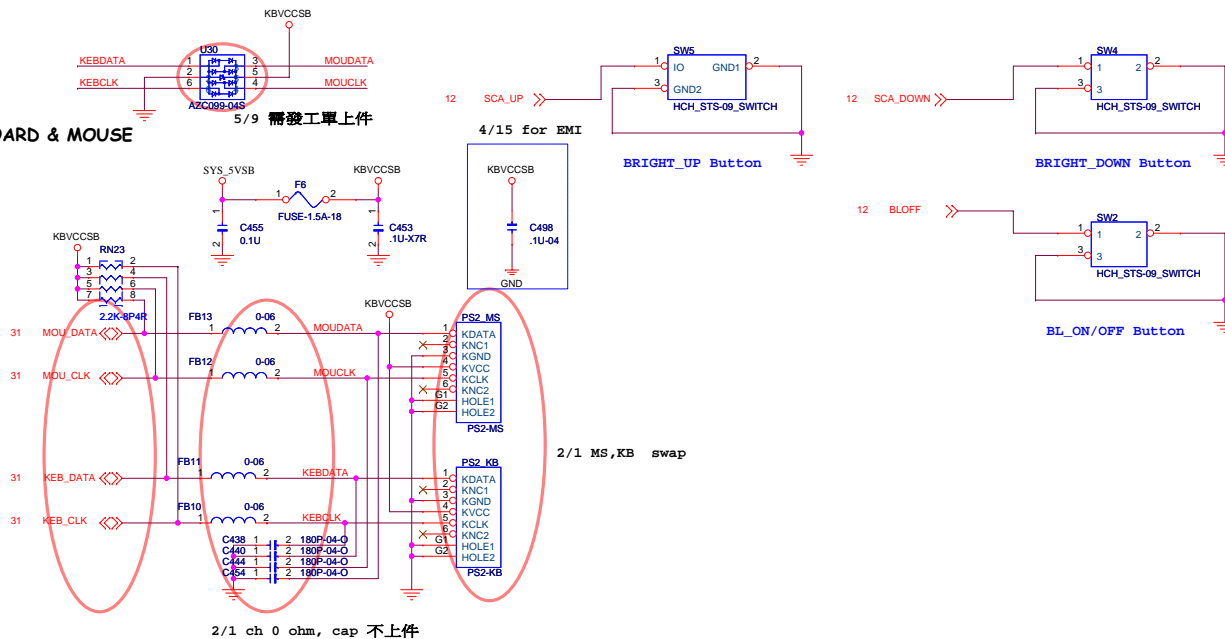
Rear Panel



0507 ADD EUP

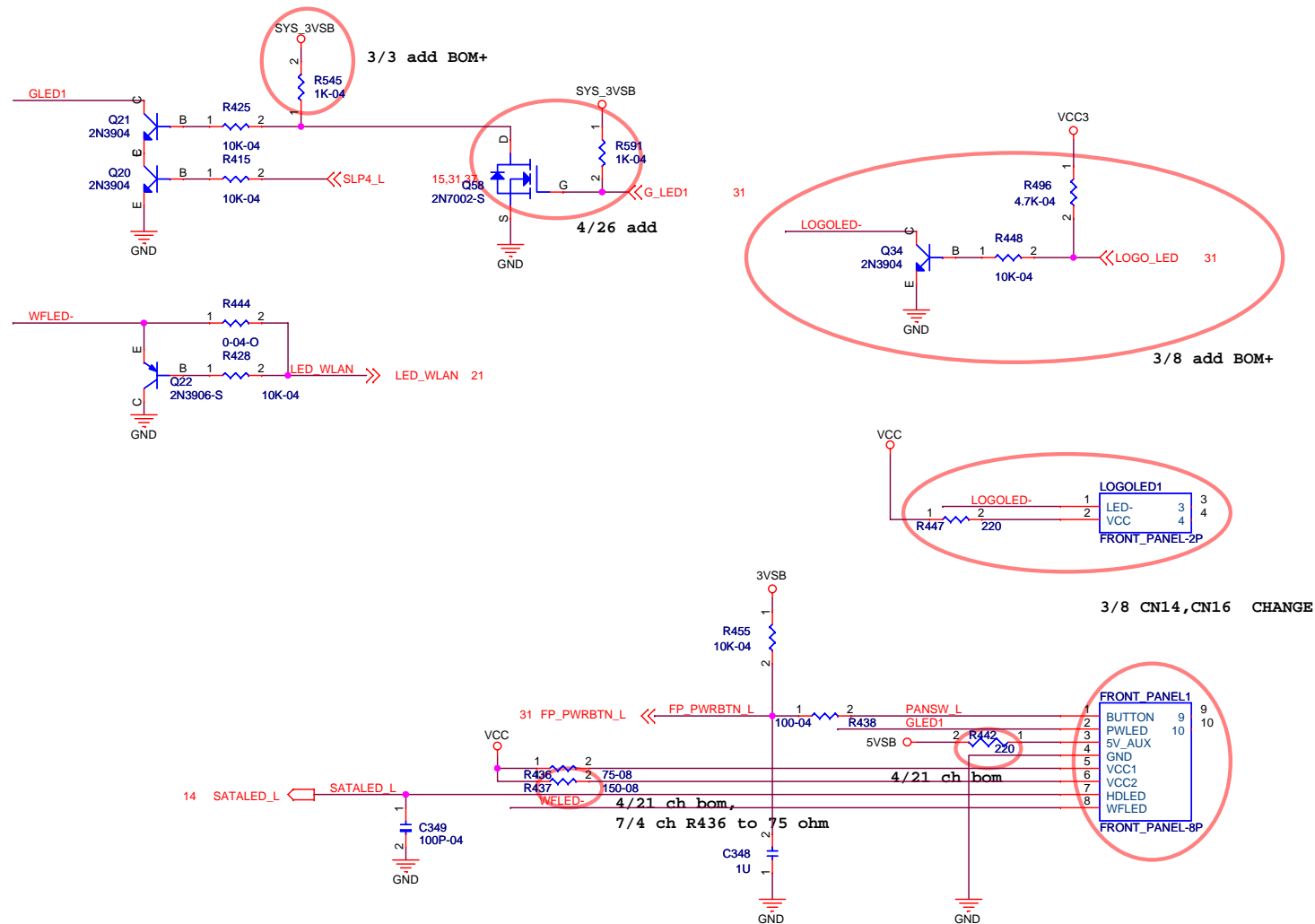


KEYBOARD & MOUSE

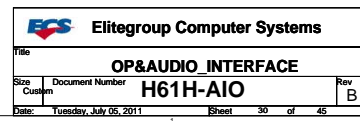


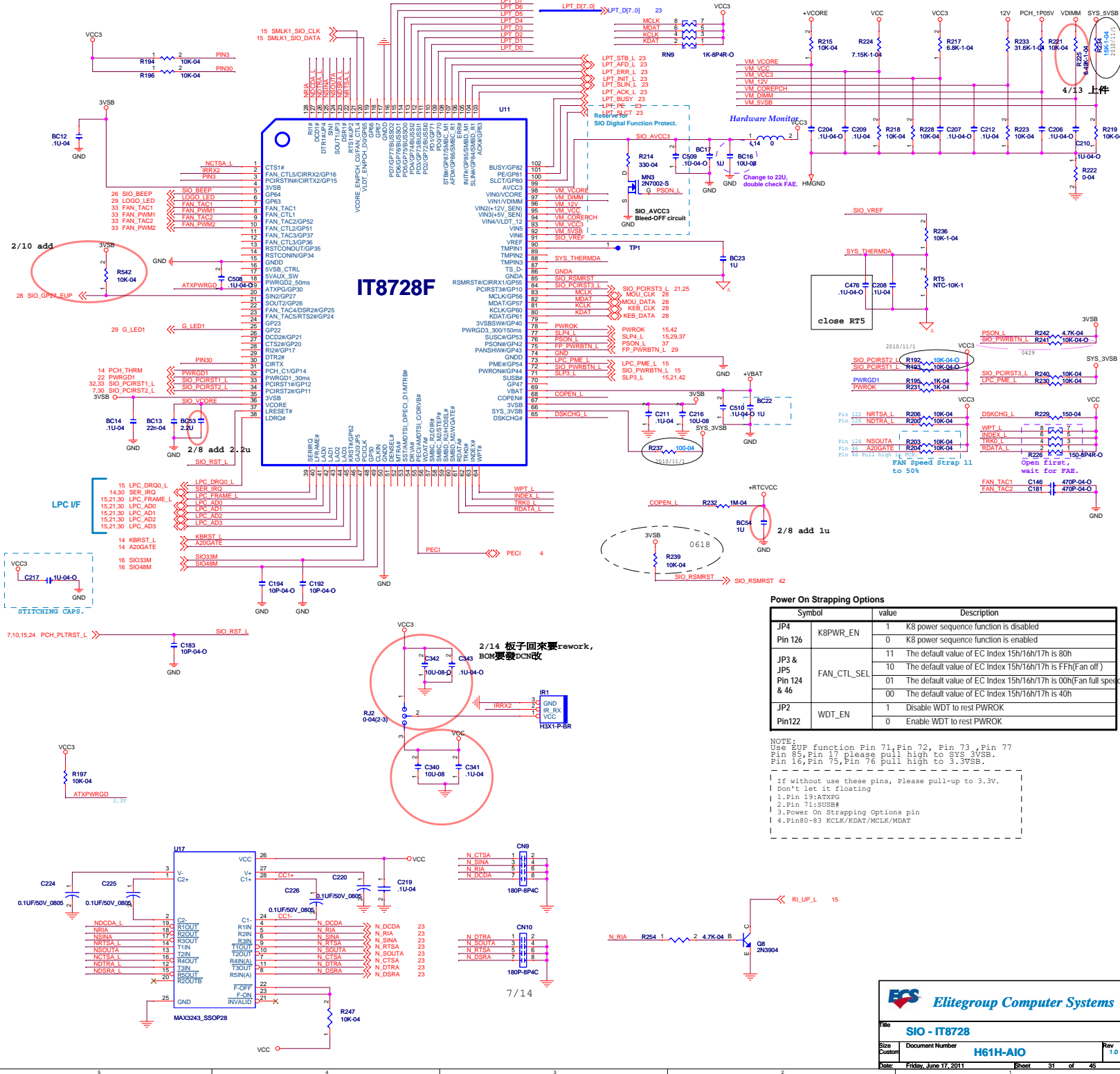
2/1 ch 0 ohm, cap 不上件

Front Panel



Title			FRONT PANEL LED	
Size	Document Number		Rev	
B	H61H-AIO		1.0	
Date:	Monday, July 04, 2011		Sheet	29 of 45



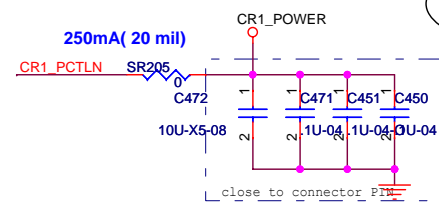
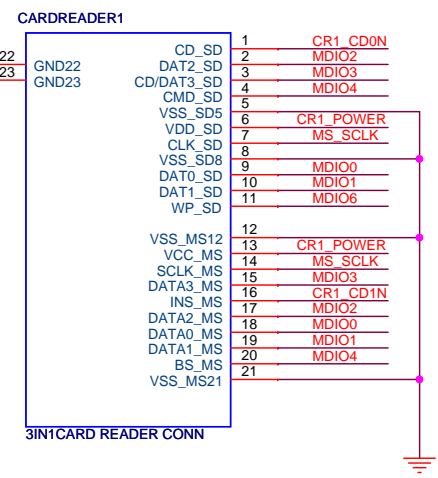
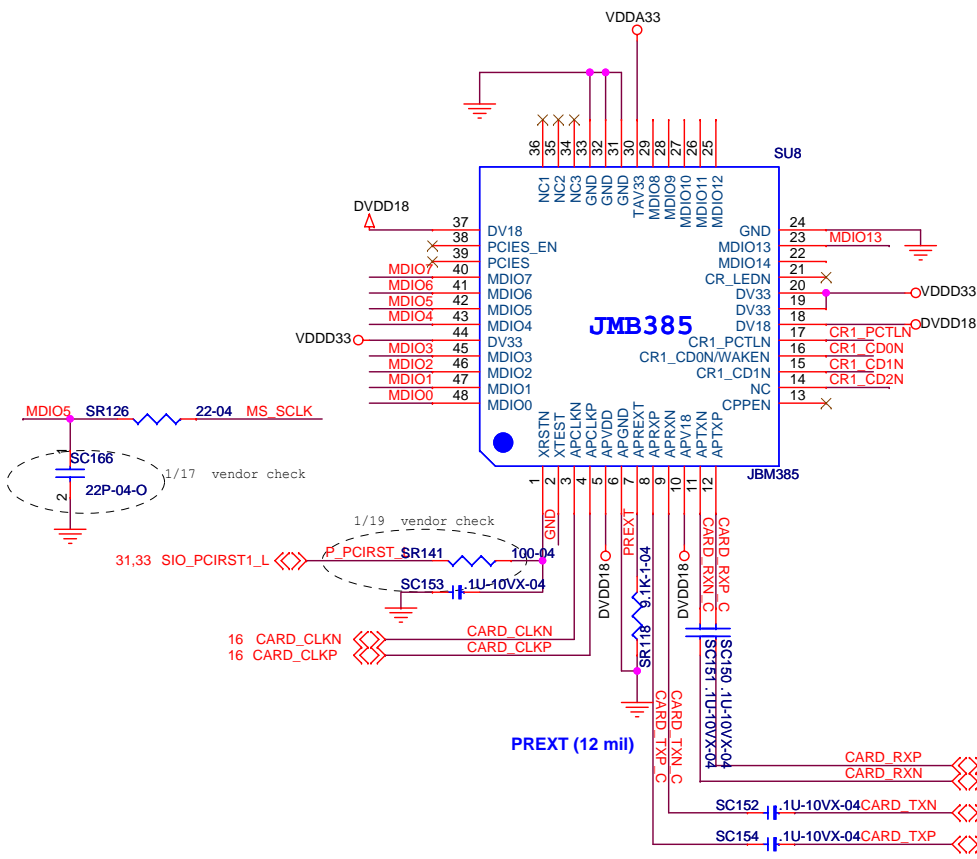


Power On Strapping Options

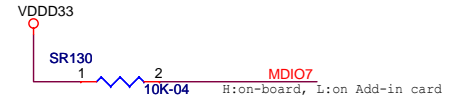
Symbol	value	Description
JP4	1	K8 power sequence function is disabled
Pin 126	0	K8 power sequence function is enabled
JP3 & JP5	11	The default value of EC Index 15h/16h/17h is 80h
Pin 124 & 46	10	The default value of EC Index 15h/16h/17h is FFh(Fan off)
	01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
	00	The default value of EC Index 15h/16h/17h is 40h
JP2	1	Disable WDT to rest PWROK
Pin122	0	Enable WDT to rest PWROK

NOTE:
Use SUP function Pin 71, Pin 72, Pin 73, Pin 77
Pin 85, Pin 17 please pull high to SYS 3VSB.
Pin 16, Pin 75, Pin 76 pull high to 3.3VSB.

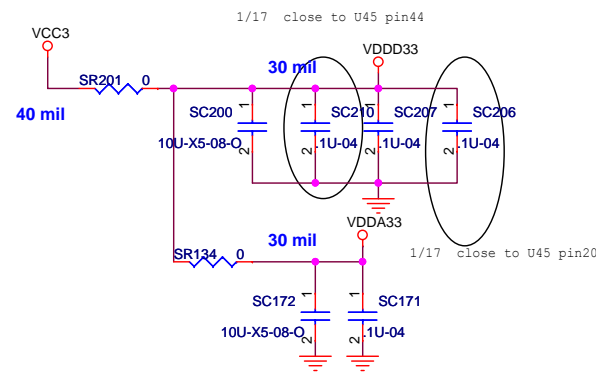
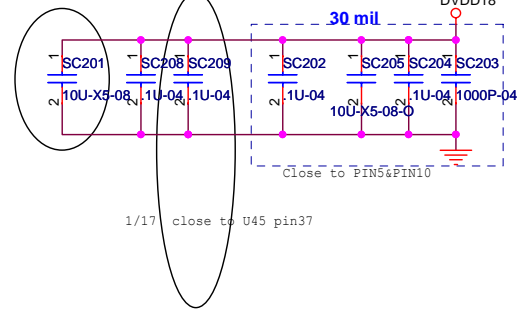
If without use these pins, Please pull-up to 3.3V.
Don't let it floating
1. Pin 19: ATXPG
2. Pin 71: SUSBP#
3. Power On Strapping Options pin
4. Pin80-83 KCLK/KDAT/MCLK/MDAT



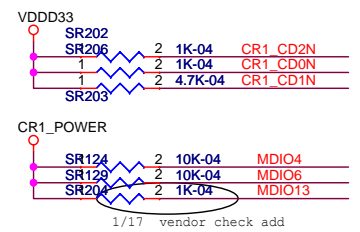
1/17 vendor check del
SBT2, SC115




1/17 vendor check close to U45 pin18



1/17 vendor check del
Reserve circuit for debugging



**Elitegroup Computer Systems**

Card reader (JMB385)

Size Custom

Document Number

Rev B

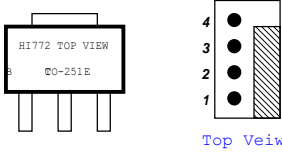
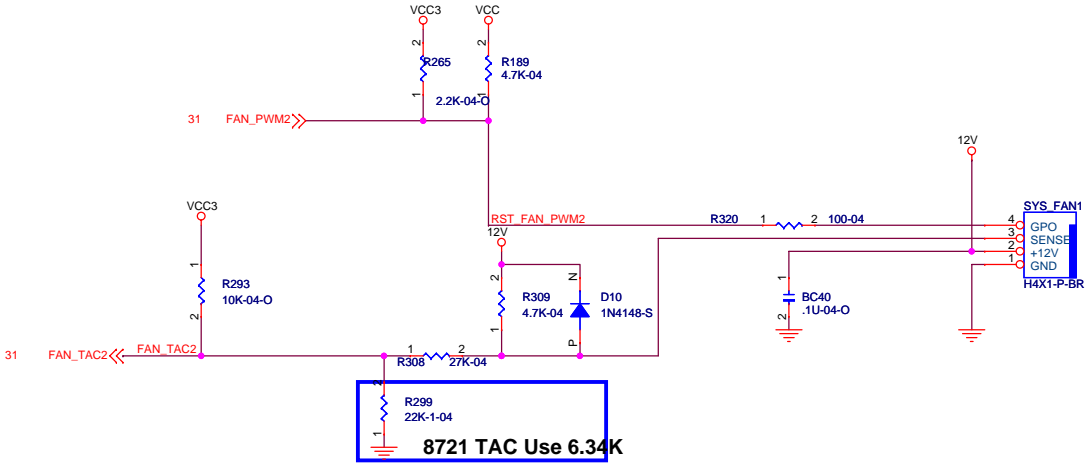
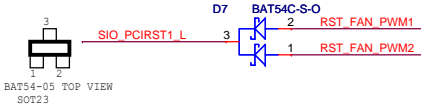
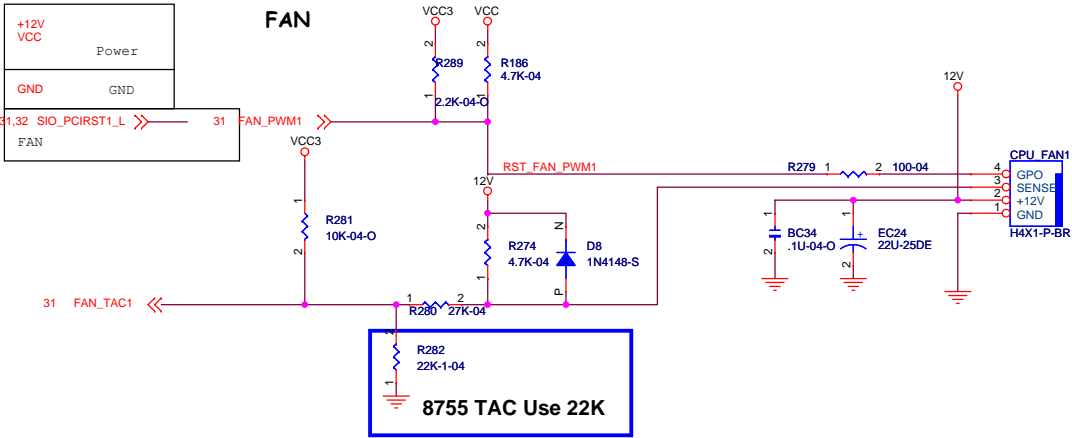
Date: Tuesday, May 17, 2011

Sheet 32 of 45

5VSB	POWER
VCC	
3VSB	
GND	GND

LABEL1

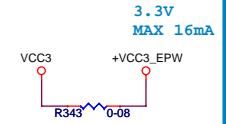
LANID



1/7 DEL


PCH_MEPWROK Circuit

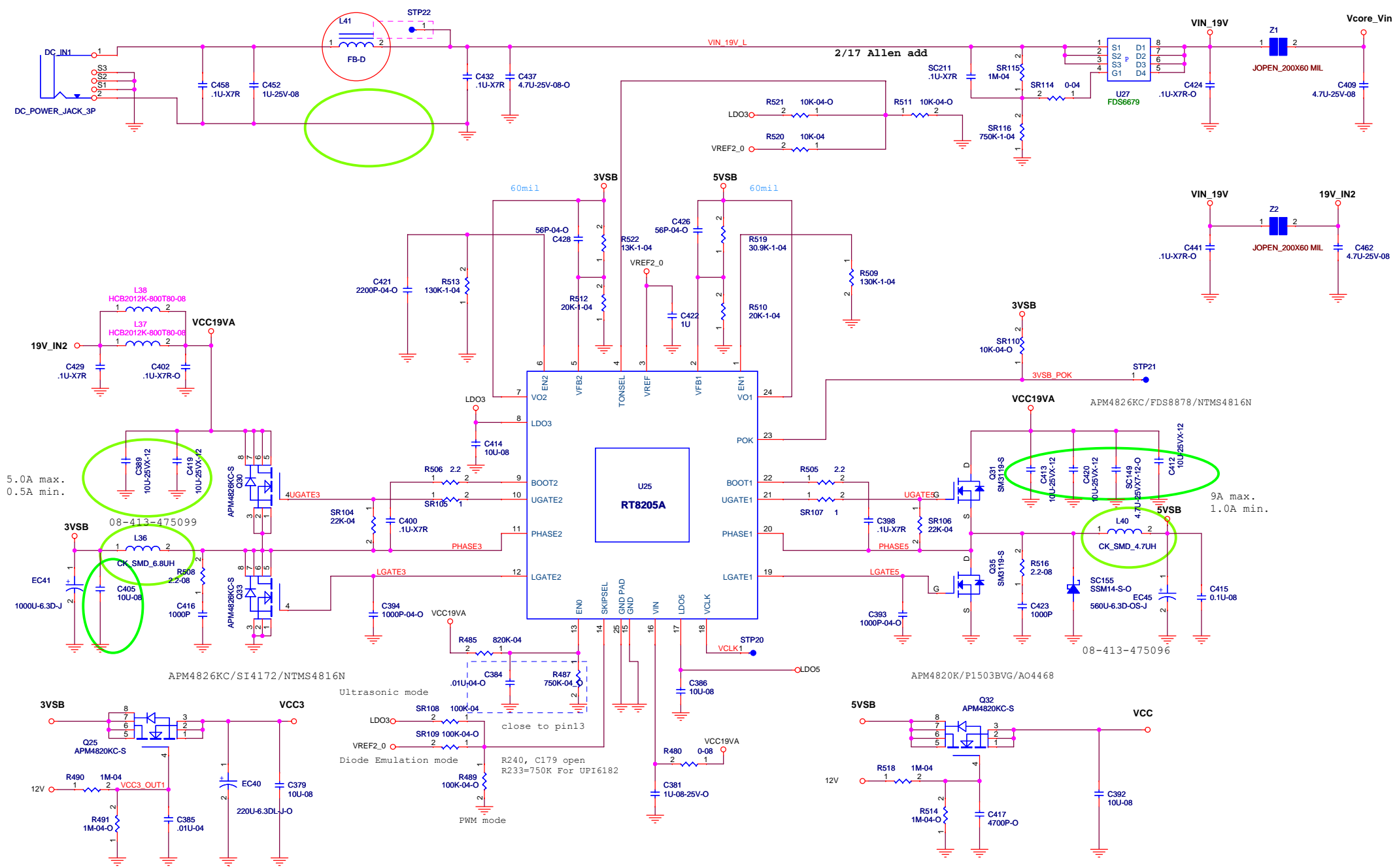
1/7 DEL



VCC3_EPW control

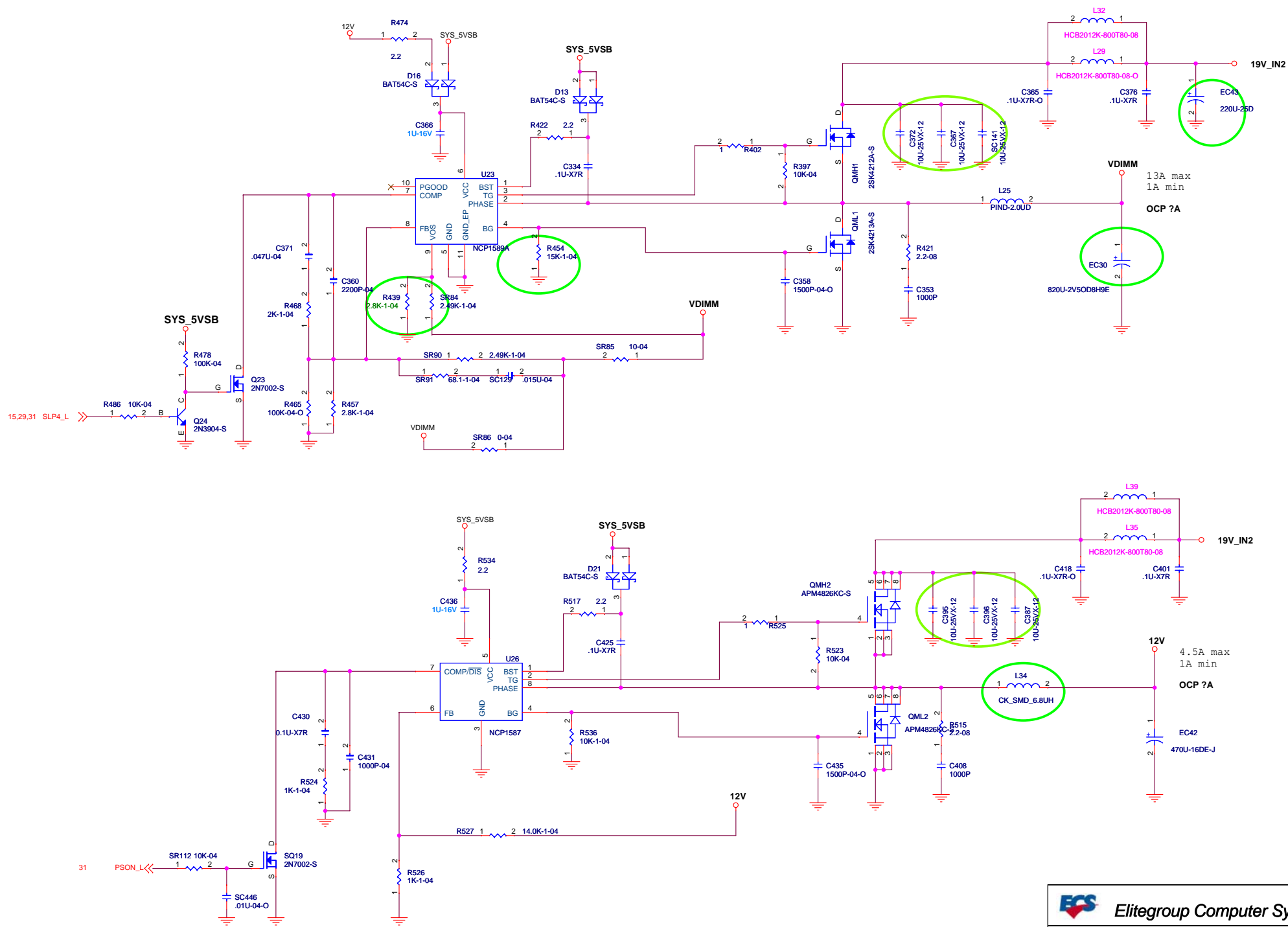
VCC3 Net to +VCC3_EPW FOR
NON-INTEL LAN (NO WOL) OR M0 ONLY

 <i>Elitegroup Computer Systems</i>	
Title DC/DC 3VDUAL	
Size Custom	Document Number H61H-AIO Rev 1.0
Date: Thursday, April 28, 2011	Sheet 34 of 45



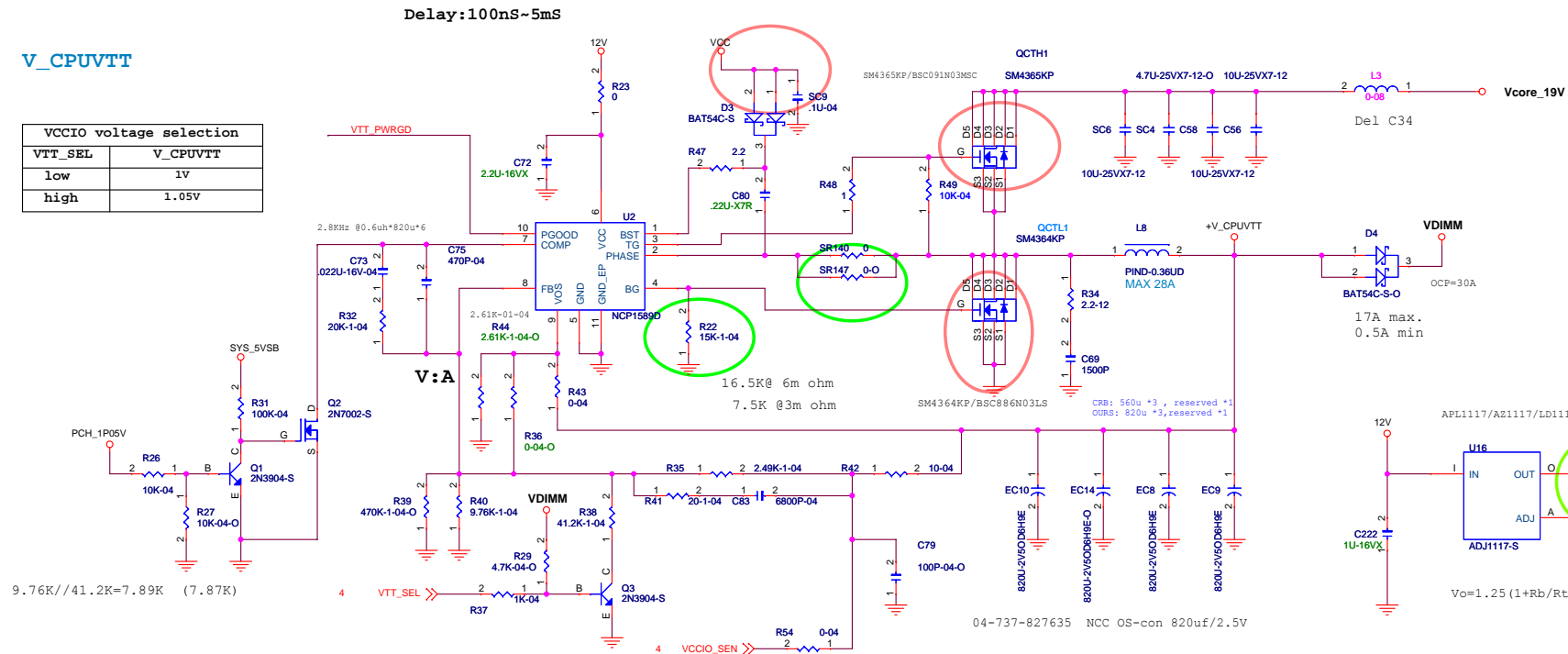
1.05V@1.7A Max





V_CPUVTT

VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V



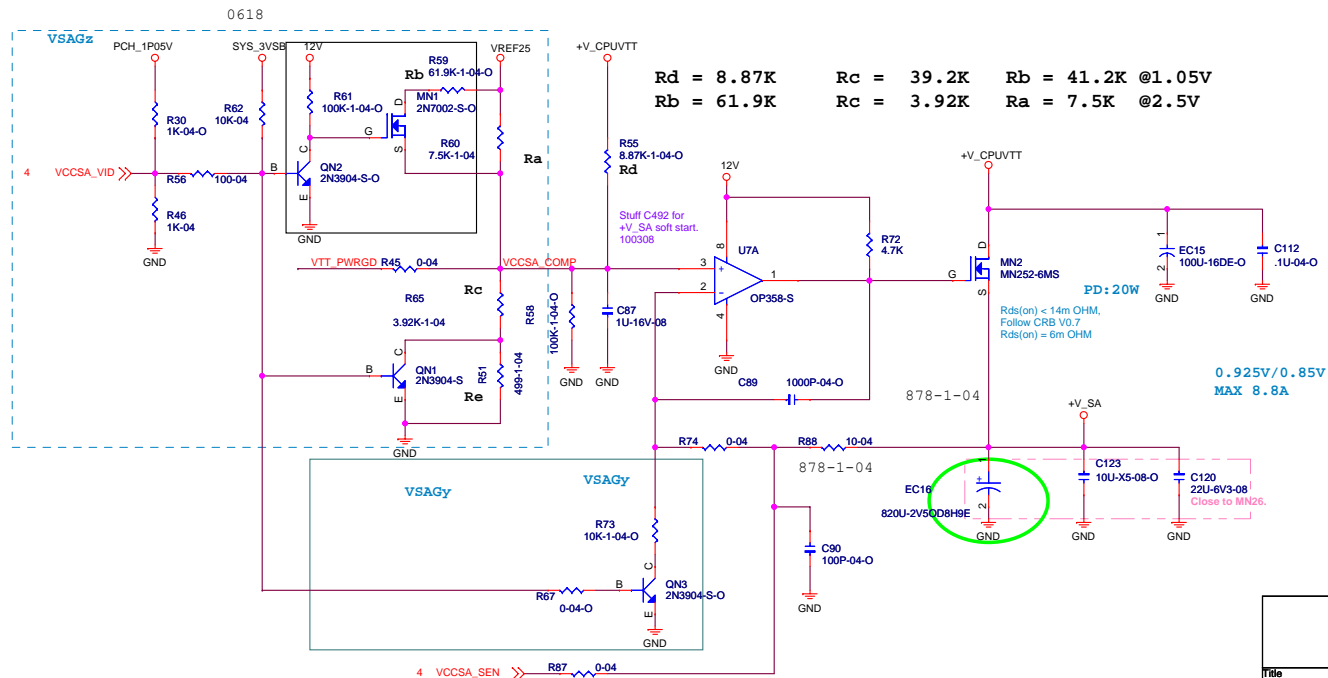
Default Stuffed:

Stuff VSAGz

VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

Stuff VSAGy

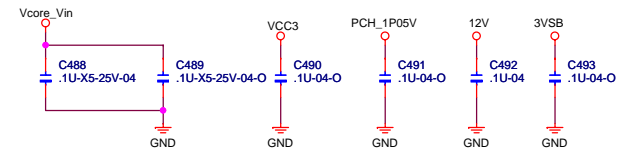
VCCSA voltage selection	
VID	+V_SA
0	0.85V
1	0.925V



Elitegroup Computer Systems

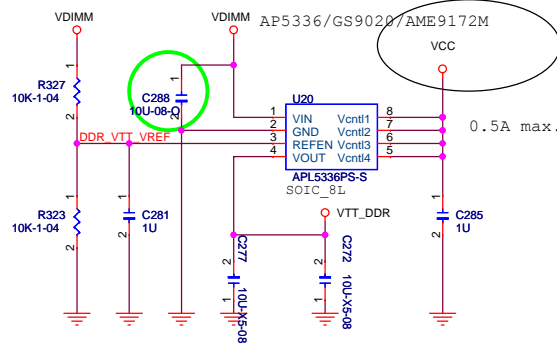
Title		DC/DC V_CPUVTT
Size	Document Number	H61H-AIO
Custom		Rev 1.0
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1/7 DEL XDP

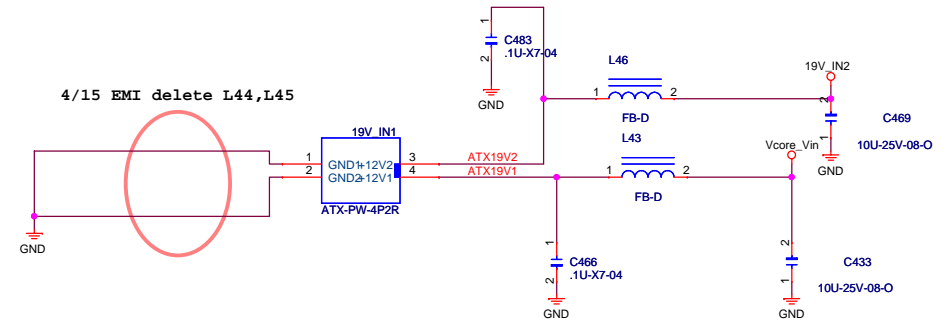


2/24 EMI add caps

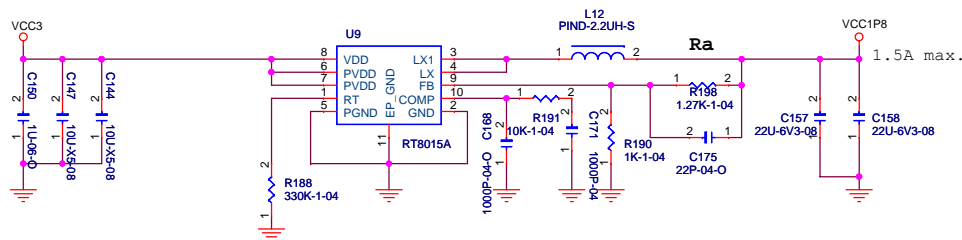
DDR VTT~0.83A (DDR3)



4/15 EMI delete L44,L45



08-463-225092
2.2uH DCR 60mOhm



NOTE:

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

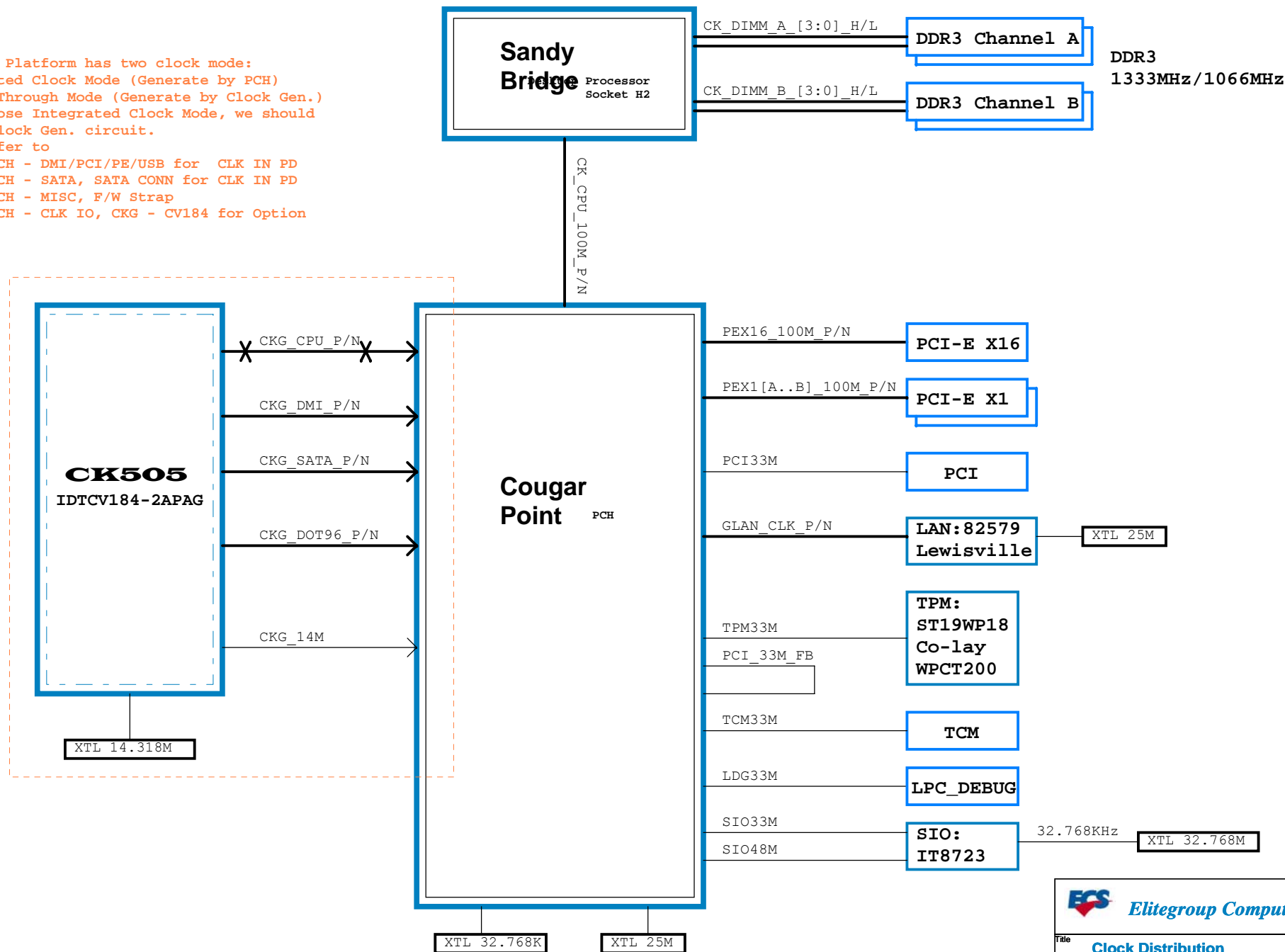
Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option



Deep Sleep S5/S4 Power sequence

